■ DESCRIPTION

The CS18LV40963 is a high performance, high speed, low power CMOS Static Random Access Memory organized as 524,288 words by 8 bits and operates from a wide range of 2.7 to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.20uA and maximum access time of 50/55/70ns in 3.0V operation. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE) and three-state output drivers.

The CS18LV40963 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS18LV40963 is available in JEDEC standard 32-pin TSOP (I) (8x20mm), TSOP (II) (400 mil), SOP (450 mil), STSOP (8x13.4 mm) and 36-ball CSP 6x8mm package..

■ FEATURES

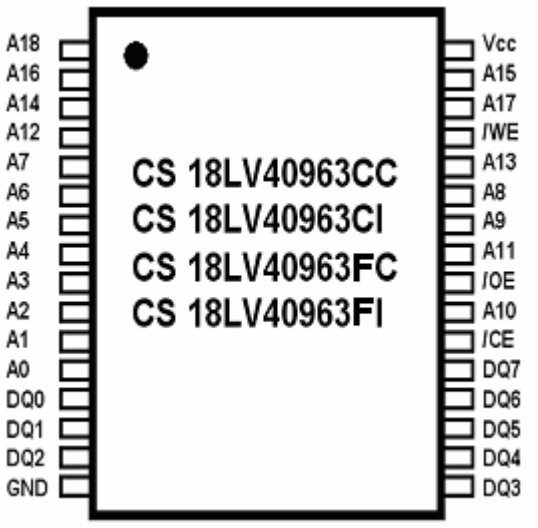
- Low operation voltage : 2.7 ~ 3.6V
  Ultra low power consumption :
  (Vcc = 3.0V) 3mA@1MHz (Max.) operating current
  0.20 uA (Typ.) CMOS standby current
- High speed access time : 50~70ns (Max.) at Vcc = 3.0V.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible
- Fully static operation.
- Data retention supply voltage as low as 1.5V.
- Easy expansion with /CE and /OE options.

■ Product Family

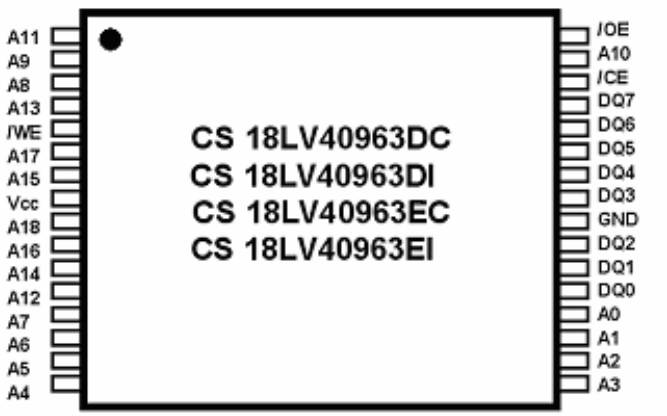
Part No.	Operating Temp	Vcc. Range	Speed (ns)	Standby (Typ.)	Package Type
CS18LV40963CC	0~70°C	2.7~3.6	50/55/70	0.20 uA (Vcc = 3.3V)	32 SOP
CS18LV40963DC					32 STSOP
CS18LV40963EC					32 TSOP (I)
CS18LV40963FC					32 TSOP (II)
CS18LV40963KC					36 CSP-0608
CS18LV40963CI	-40~85°C	2.7~3.6	50/55/70	0.30 uA (Vcc= 3.3V)	32 SOP
CS18LV40963DI					32 STSOP
CS18LV40963EI					32 TSOP (I)
CS18LV40963FI					32 TSOP (II)
CS18LV40963KI					36 CSP-0608

Note: Green package part no, sees order information.

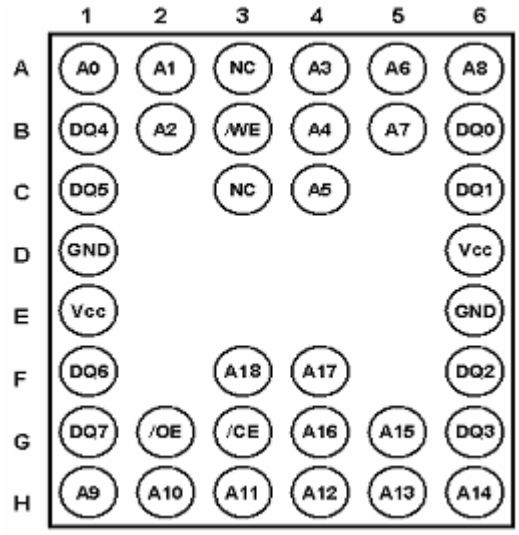
■ PIN CONFIGURATIONS



32 SOP 450 mil
32 TSOP(II) 400 mil

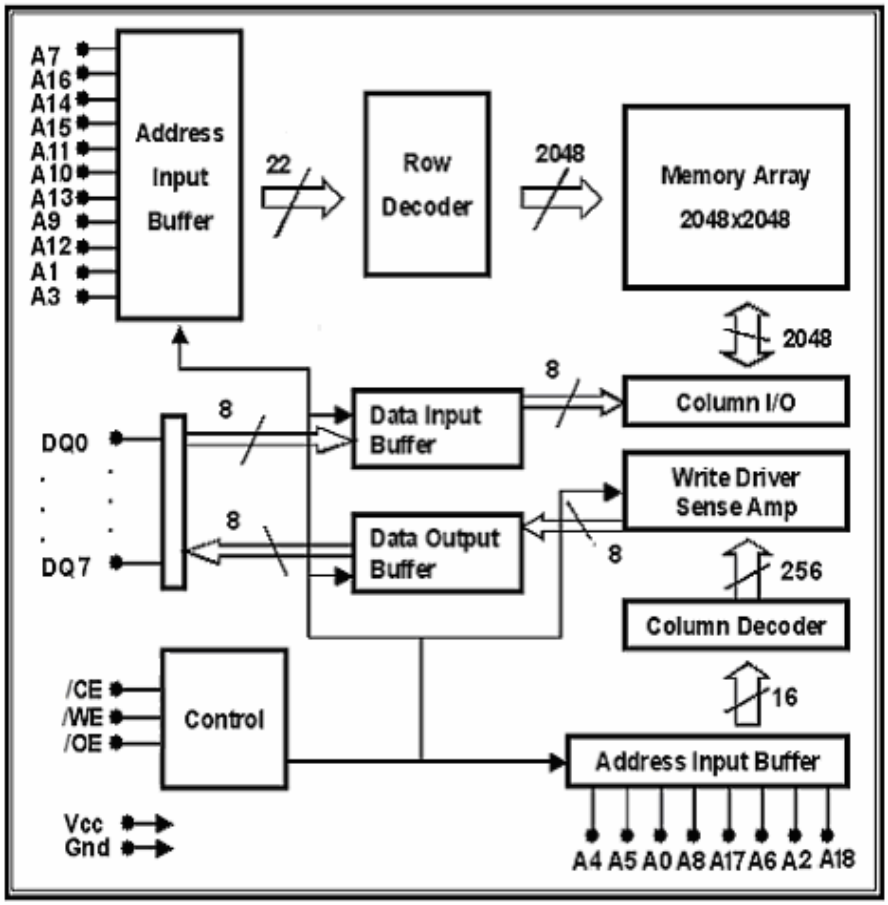


32 STSOP 8x13.4mm
32 TSOP(I) 8x20mm



36 Ball CSP – Top View

BLOCK DIAGRAM



■ PIN DESCRIPTIONS

Name	Function
A0-A18 **Address Input**	These 19 address inputs select one of the 524,288 x 8-bit words in the RAM.
/CE **Chip Enable Input**	/CE is active LOW Chip enables must be active when data read from or write to the device. if chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
/WE **Write Enable Input**	The write enable input is active LOW and controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins; when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE **Output Enable Input**	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
DQ0-DQ7 **Data Input/Output Ports**	These 8 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power Supply
Gnd	Ground

■ TRUTH TABLE

MODE	/CE	/WE	/OE	DQ0~7	Vcc Current
Not Selected	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
	X	X	X		
Output Disabled	L	H	H	High Z	I_{CC}
Read	L	H	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

■ ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +125	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ DC ELECTRICAL CHARACTERISTICS (TA = 0 to + 70°C , Vcc = 3.0V)

Parameter Name	Parameter	Test Conduction	MIN	TYP(1)	MAX	Unit
V_{IL}	Guaranteed Input Low Voltage (2)		-0.5		0.8	V
V_{IH}	Guaranteed Input High Voltage (2)		2.0		Vcc+0.2	V
I_{IL}	Input Leakage Current	V_{CC}=MAX, V_{IN}=0 to V_{CC}			1	uA
I_{OL}	Output Leakage Current	V_{CC}=MAX, /CE=V_{IN}, or /OE=V_{IN} , V_{IO}=0V to V_{CC}			1	uA
V_{OL}	Output Low Voltage	V_{CC}=MAX, I_{OL} = 2mA			0.4	V
V_{OH}	Output High Voltage	V_{CC}=MIN, I_{OH} = -1mA	2.4			V
I_{CC}	Operating Power Supply Current	/CE=V_{IL}, I_{DQ}=0mA, F=F_{MAX}(3)			30	mA
I_{CCSB}	Standby Supply - TTL	/CE=V_{IH}, I_{DQ}=0mA,			1	mA
I_{CCSB1}	Standby Current -CMOS	/CE≧V_{CC}-0.2V, V_{IN}≧ V_{CC}-0.2V or V_{IN}≦0.2V		0.2	3	uA

1. Typical characteristics are at TA = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.
3. Fmax = $1/t_{RC}$.

■ OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0~70°C	2.7V ~ 3.6V
Industrial	-40~85°C	2.7V ~ 3.6V

■ DATA RETENTION CHARACTERISTICS (TA = 0 to + 70°C , Vcc = 3.0V)

Parameter Name	Parameter	Test Conduction	MIN	TYP(1)	MAX	Unit
V_{RD}	V_{CC} for Data Retention	/CE≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V	1.5			V
I_{CCDR}	Data Retention Current	/CE≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V		0.1	1	uA
T_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0			ns
t_R	Operation Recovery Time		t_{RC} (2)			ns

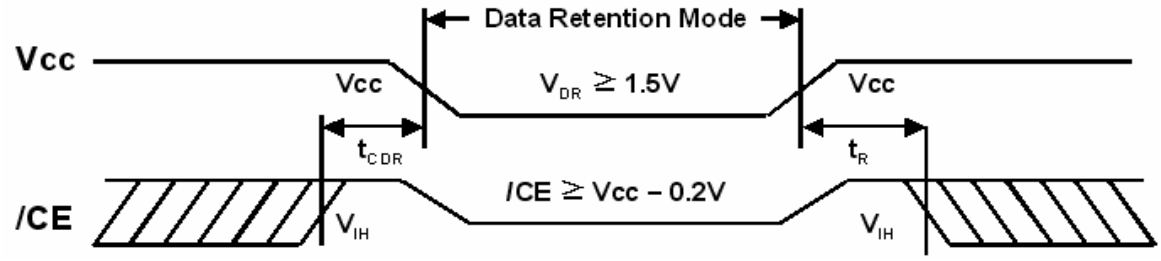
1. Vcc = 3.0V, TA = + 25°C.
2. = Read Cycle Time.

■ CAPACITANCE (1) (TA = 25°C, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	10	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$=0V	10	pF

1. This parameter is guaranteed and not tested.

■ LOW Vcc DATA RETENTION WAVEFORM (/CE Controlled)



■ AC TEST CONDITIONS

Input Pulse Levels	Vcc/0V
Input Rise and Fall Times	5ns
Input and Output	
Timing Reference Level	0.5Vcc

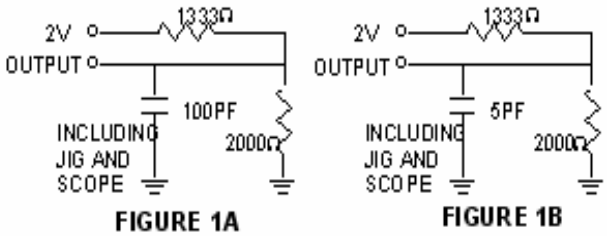


FIGURE 1A FIGURE 1B

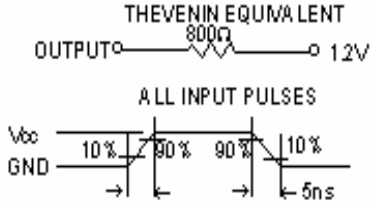


FIGURE 2

■ KEY TO SWITCHING WAVEFORMS

WAFEFORM	INPUTS	OUTPUTS
	Must be standby	Must be standby
	May change for H to L	Will be change from H to L
	May change for L to H	May change for L to H
	Don’t care any change permitted	Change state unknown
	Does not apply	Center line is high impedance “OFF” state

■ AC ELECTRICAL CHARACTERISTICS (TA = 0 to + 70°C , Vcc = 3.3V)

< READ CYCLE >

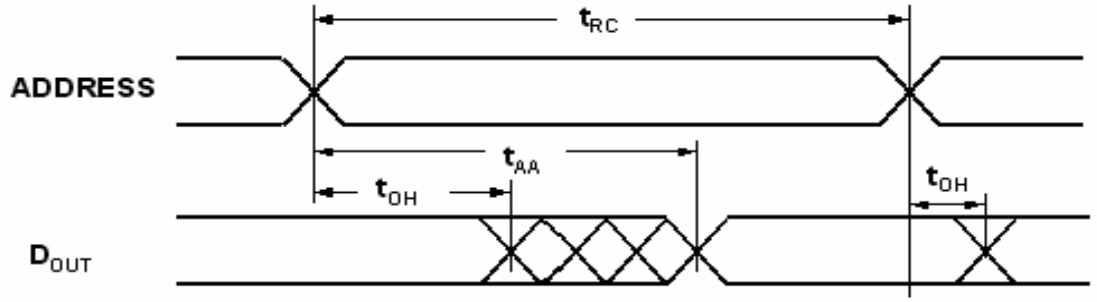
JEDEC Parameter Name	Parameter Name	Description	-50/55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{RC}	Read Cycle Time	50/55		70		ns
t_{AVQV}	t_{AA}	Address Access Time		50/55		70	ns
t_{ELQV}	t_{ACS}	Chip Select Access Time (/CE)		50/55		70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		25		35	ns
t_{ELQX}	t_{CLZ}	Chip Select to Output Low Z (/CE)	10		10		ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		5		ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z (/CE)	0	25	0	30	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	25	0	30	ns
t_{AXOX}	t_{OH}	Out Disable to Address Change	10		10		ns

NOTES:

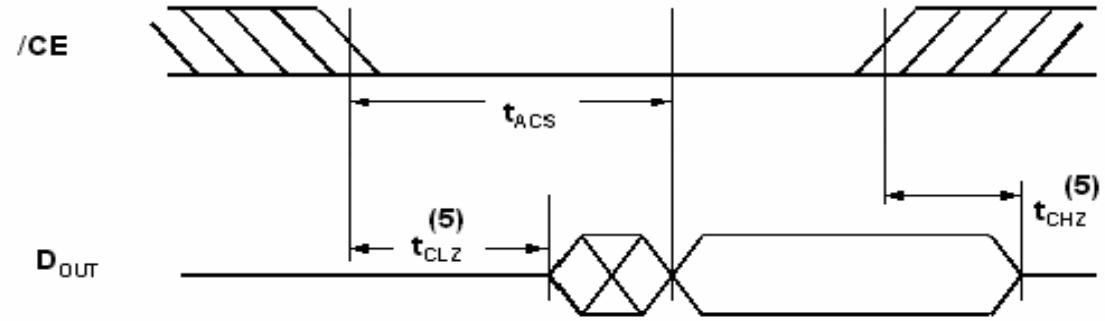
1. /WE is high in read Cycle.
2. Device is continuously selected when /CE = $V_{IL.}$
3. Address valid prior to or coincident with CE transition low.
4. /OE = VIL.
5. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.

■ SWITCHING WAVEFORMS (READ CYCLE)

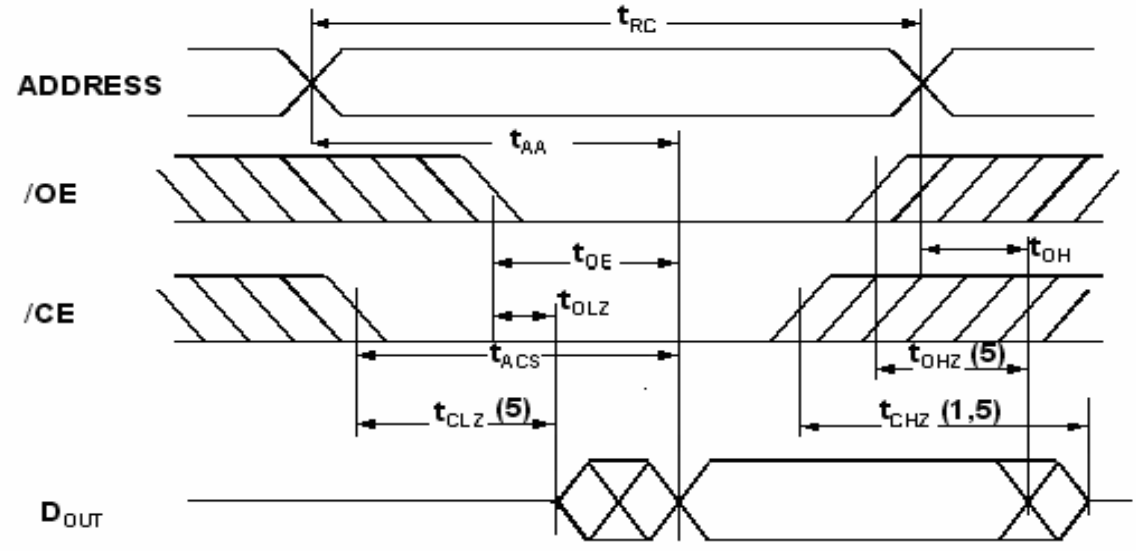
READ CYCLE 1 (1,2,4)



READ CYCLE 2 (1,3,4)



READ CYCLE 3 (1,4)



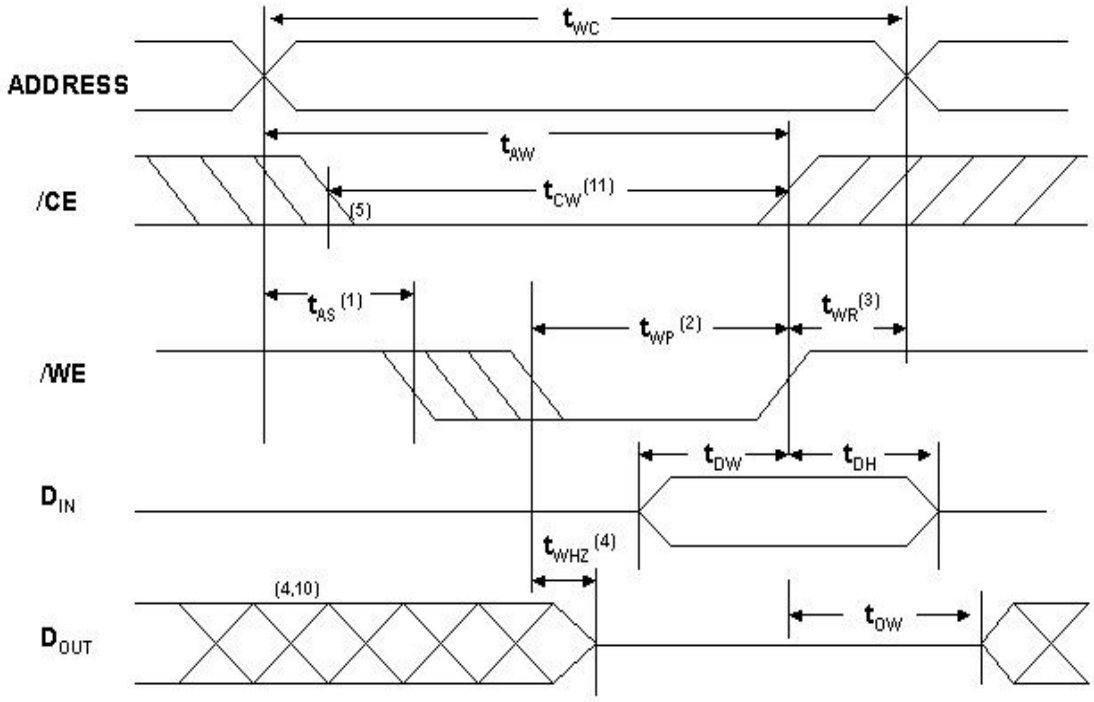
■ AC ELECTRICAL CHARACTERISTICS (TA = 0 to + 70°C , Vcc = 3.3V)

< WRITE CYCLE >

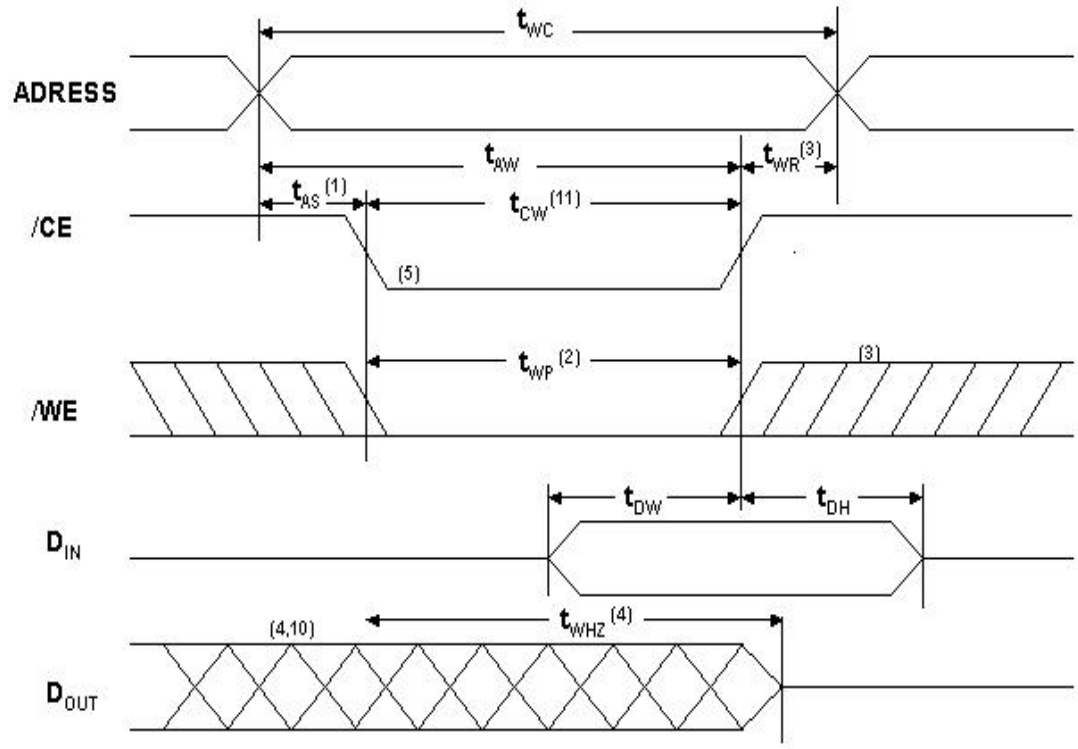
JEDEC Parameter Name	Parameter Name	Description	-50/55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{WC}	Write Cycle Time	50/55		70		ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	50		60		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	50/55		60		ns
t_{WLWH}	t_{WP}	Write Pulse Width	45		50		ns
t_{WHAX}	t_{WR}	Write Recovery Time (/CE, /WE)	0		0		ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		20		25	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	25		30		ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0		0		ns
t_{WHOX}	t_{OW}	End of Write to Output Active	5		10		ns

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1 (Write Enable Controlled)



WRITE CYCLE 2 (Chip Enable Controlled)



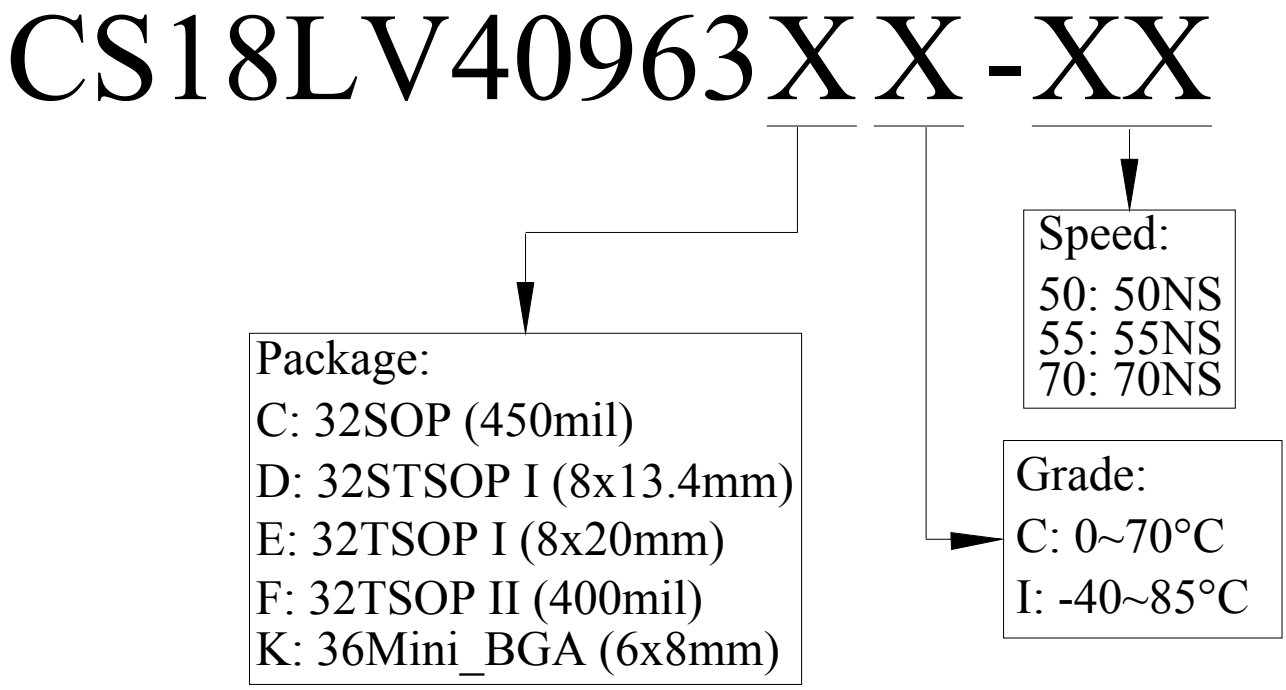
NOTES:

1. T_{AS} is measured from the address valid to the beginning of write.
2. The internal write time of the memory is defined by the overlap of /CE and /WE low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of /CE or /WE going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the /CE low transition occurs simultaneously with the /WE low transitions or after the /WE transition, output remain in a high impedance state.

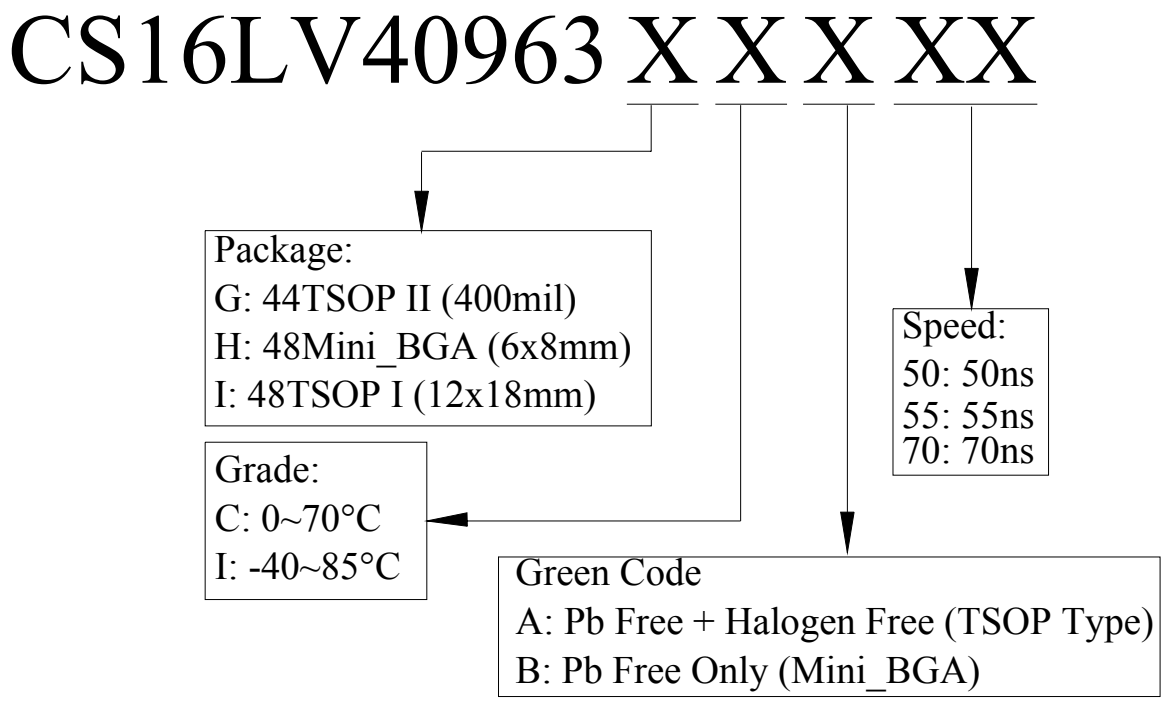
6. /OE is continuously low (/OE = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If /CE is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of /CE going low to the end of write.

■ ORDER INFORMATION

1. NON-GREEN PACKAGE:

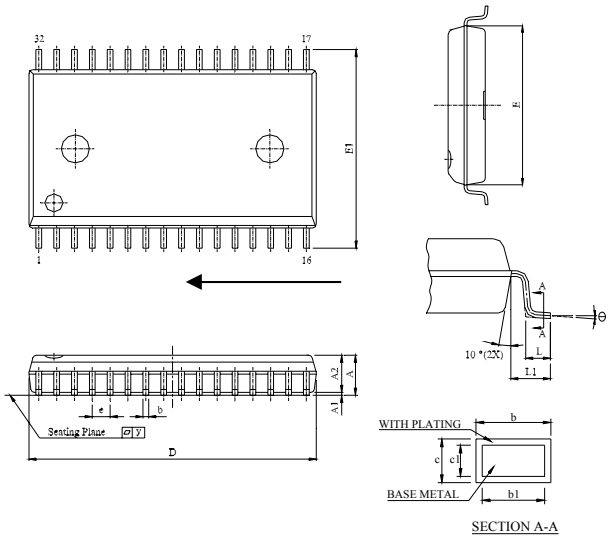


2. GREEN PACKAGE:



■ PACKAGE DIMENSIONS

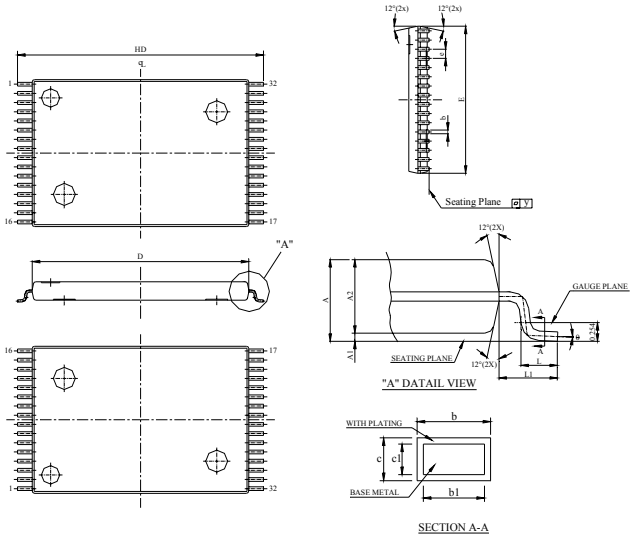
- **32 pin SOP (450 mil) :**



SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	Θ
mm	Min.	2.645	0.102	2.540	0.35	0.35	0.15	0.15	20.320	11.176	13.792	1.118	0.584	1.194	–	0°
	Nom.	2.821	0.229	2.680	–	–	–	–	20.447	11.303	14.097	1.270	0.834	1.397	–	–
	Max.	2.997	0.356	2.820	0.50	0.46	0.32	0.28	20.574	11.430	14.402	1.422	1.084	1.600	0.1	10°
inch	Min.	0.104	0.004	0.1000	0.014	0.014	0.006	0.006	0.800	0.440	0.543	0.044	0.023	0.047	–	0°
	Nom.	0.111	0.009	0.1055	–	–	–	–	0.805	0.445	0.555	0.050	0.033	0.055	–	–
	Max.	0.118	0.014	0.1110	0.020	0.018	0.012	0.011	0.810	0.450	0.567	0.056	0.043	0.063	0.004	10°

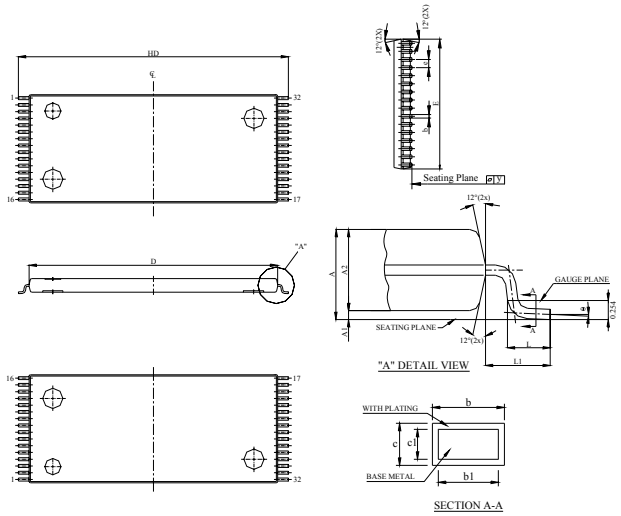
-

- **32 pin sTSOP (8x13.4 mm) :**



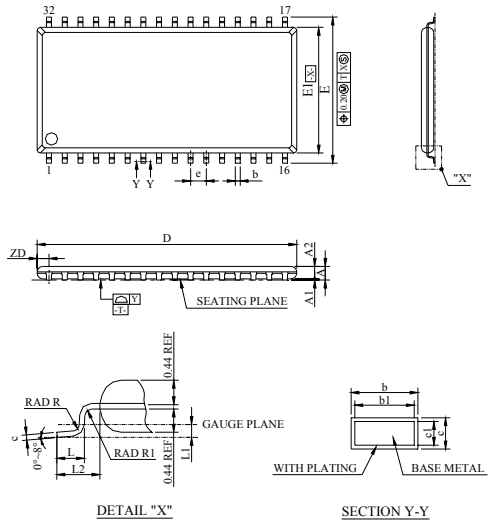
SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	Θ
mm	Min.	1.00	0.05	0.95	0.17	0.17	0.10	0.10	11.70	7.90	0.40	13.20	0.40	0.70	–	0°
	Nom.	1.10	0.10	1.00	0.22	0.20	–	–	11.80	8.00	0.50	13.40	0.50	0.80	–	–
	Max.	1.20	0.15	1.05	0.27	0.23	0.21	0.16	11.90	8.10	0.60	13.60	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.007	0.007	0.004	0.004	0.461	0.311	0.016	0.520	0.0157	0.0275	–	0°
	Nom.	0.0433	0.004	0.039	0.009	0.008	–	–	0.465	0.315	0.020	0.528	0.0197	0.0315	–	–
	Max.	0.0473	0.006	0.041	0.011	0.009	0.008	0.006	0.469	0.319	0.024	0.536	0.0277	0.0355	0.004	8°

- **32 pin TSOP (I) (8x20 mm)**



SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	⊙
mm	Min.	1.00	0.05	0.95	0.17	0.17	0.10	0.10	18.30	7.90	0.40	19.80	0.40	0.70	–	0°
	Nom.	1.10	0.10	1.00	0.22	0.20	–	–	18.40	8.00	0.50	20.00	0.50	0.80	–	–
	Max.	1.20	0.15	1.05	0.27	0.23	0.21	0.16	18.50	8.10	0.60	20.20	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.007	0.007	0.004	0.004	0.720	0.311	0.016	0.779	0.0157	0.0275	–	0°
	Nom.	0.0433	0.004	0.039	0.009	0.008	–	–	0.724	0.315	0.020	0.787	0.0197	0.0315	–	–
	Max.	0.0473	0.006	0.041	0.011	0.009	0.008	0.006	0.728	0.319	0.024	0.795	0.0277	0.0355	0.004	8°

- **32 pin TSOP (II) 400 mil**



SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	L2	R	R1	ZD	Y
mm	Min.	–	0.05	0.95	0.30	0.30	0.12	0.10	20.82	11.56	10.03	1.27 bsc	0.40	0.25 bsc	0.8 ref	0.12	0.12	0.95 ref	–
	Nom.	–	0.10	1.00	–	0.40	–	0.127	20.95	11.76	10.16		0.50			–	–		–
	Max.	1.20	0.15	1.05	0.52	0.45	0.21	0.16	21.08	11.96	10.29		0.60			0.25	–		0.10
inch	Min.	–	0.002	0.037	0.012	0.012	0.005	0.004	0.820	0.455	0.394	0.050 bsc	0.016	0.010 bsc	0.031 ref	0.005	0.005	0.037 ref	–
	Nom.	–	0.004	0.039	–	0.016	–	0.005	0.825	0.463	0.400		0.020			–	–		–
	Max.	0.047	0.006	0.042	0.020	0.018	0.008	0.006	0.830	0.471	0.405		0.024			0.010	–		0.004

- **36-ball CSP 6x8mm**