SSD1655

Advanced Information

240 x 96 Bistable Display Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SOLOMON SYSTECH

Amendment history of SSD1655 Specification

Revision	Description of any change	Effective
1.0	1st Release to Advance Information	19-Jul-16

CONTENTS

1 GENERAL DESCRIPTION

SSD1655 is a CMOS display driver with controller for dot matrix type bistable display. It supports resolution of 240 segments x 96 commons outputs with display RAM embedded.

SSD1655 is built with SPI interface to communicate with host MCU.

2 FEATURES

- Resolution:
  - 240 Segments x 96 Commons;
- Power supply
  - VCI: 2.0 to 3.8V
  - VDD: 1.8V typical (Logic operation, generate from VDD regulator)
  - VDDIO: VDD to VCI (MCU interface logic level)
  - V0: 8.25 to 40V (High voltage panel driving, generate from charge pump)
  - VPP: 7.5V typical (For OTP programming)

- Built in inductor type booster controller with max output voltage 40V
- Internal Graphic Display memory for image buffer with size
  - 240x96/8 = 2880 bytes
- SPI MCU Interface for access registers, display memory and OTP
  - CS# (Chip select), SCLK (clock), SI (data input) and SO (data output)
  - ACK pin indicates the status of the chip.
- Flexible driving waveform defined by LUT, allowing variation on time and voltage.
- 4K-bit OTP for LUT (469 Byte for waveform LUT)
- Built in oscillator for charge pump and waveform timing. With option to use external clock supply.
- Column remap and row remap function
- Programmable MUX ratio
- Gold bump die

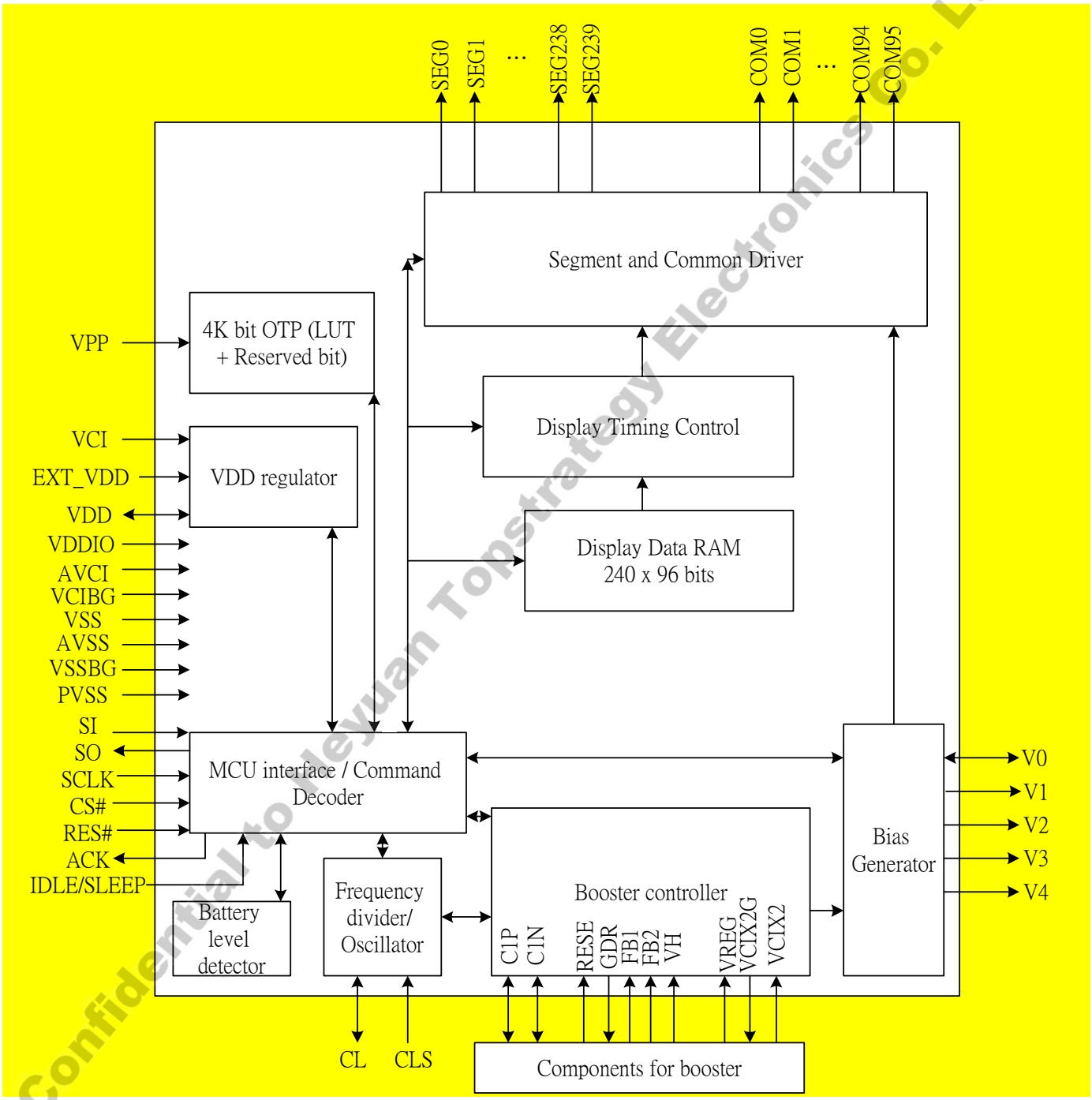
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	Package Form	Remark
SSD1655Z	Gold bumped die	–

4 BLOCK DIAGRAM

Figure 4-1 SSD1655 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1 SSD1655 layout diagram (Pad face up)

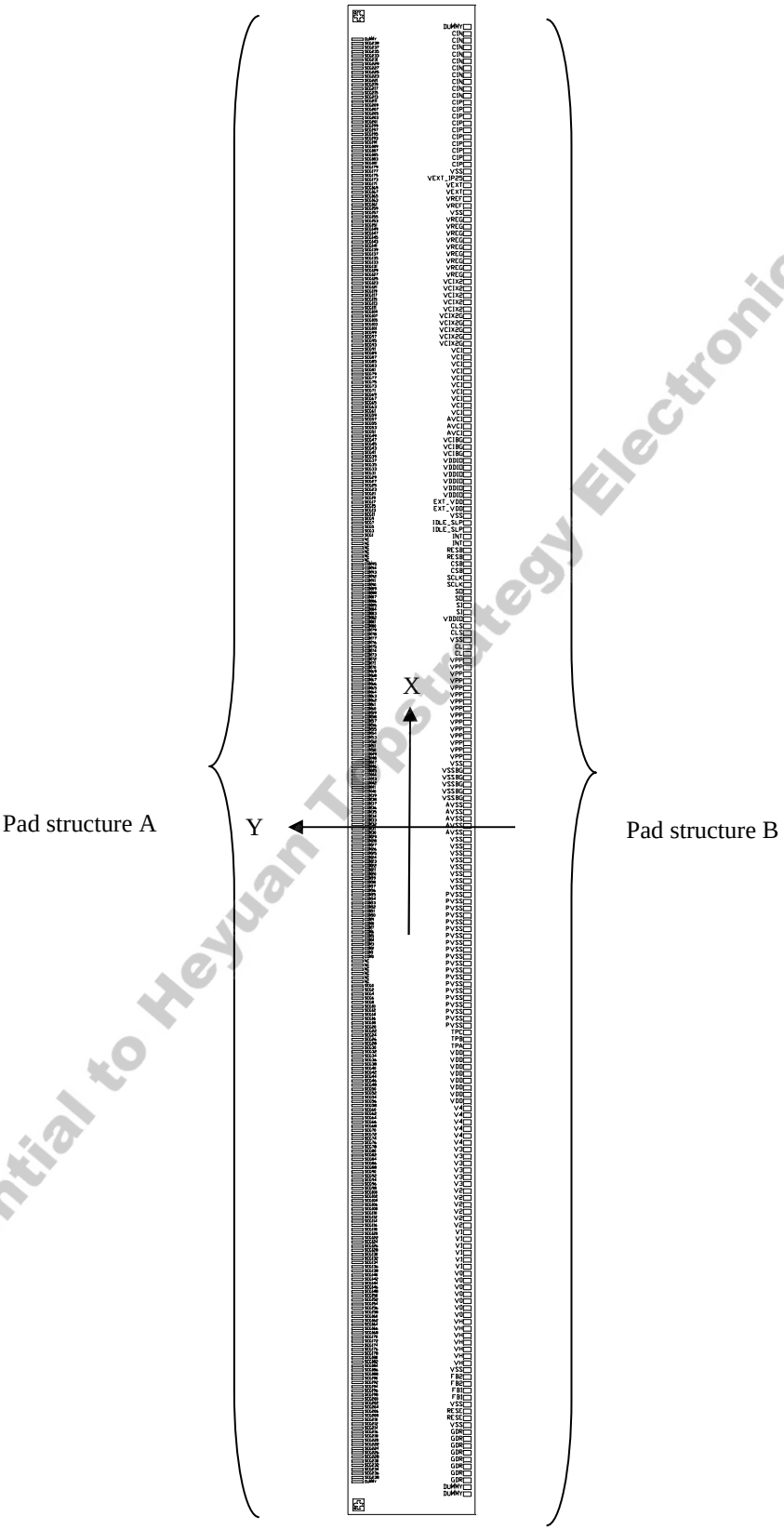


Figure 5-2 SSD1655Z -Alignment mark

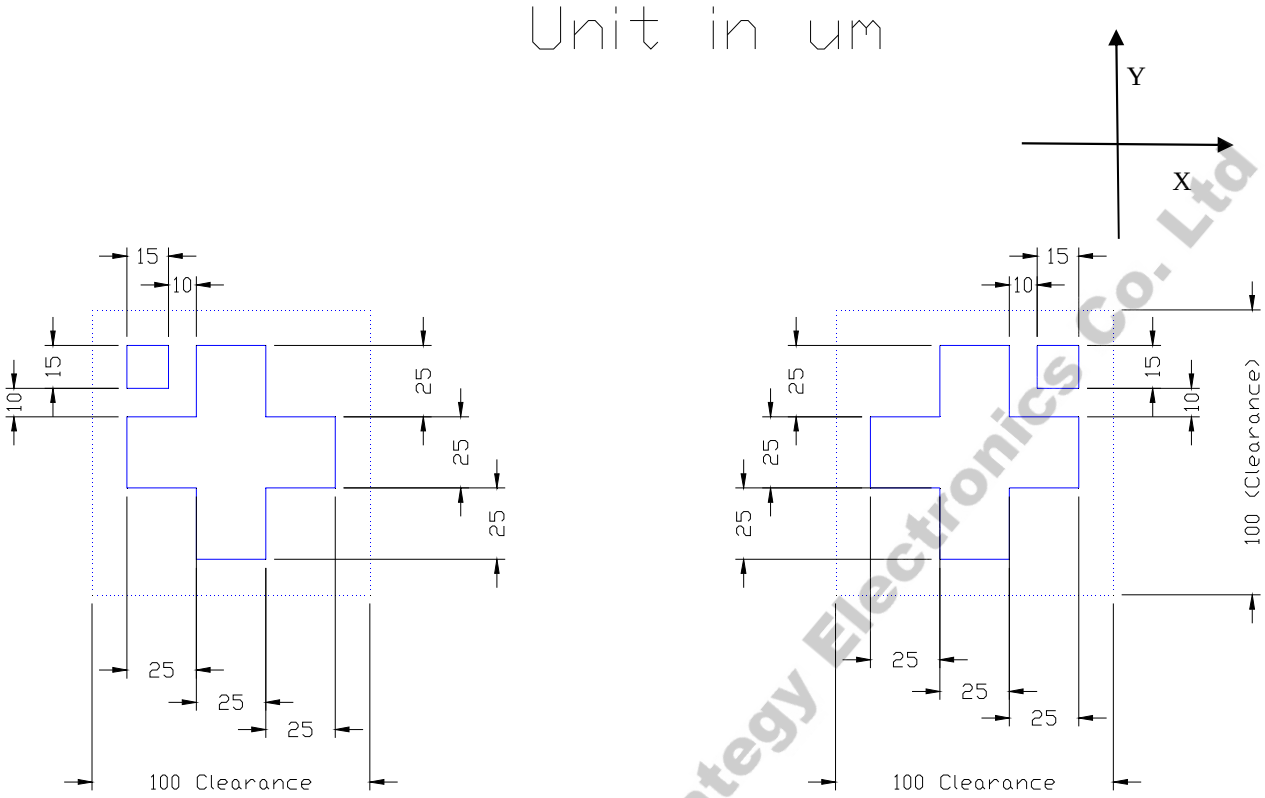
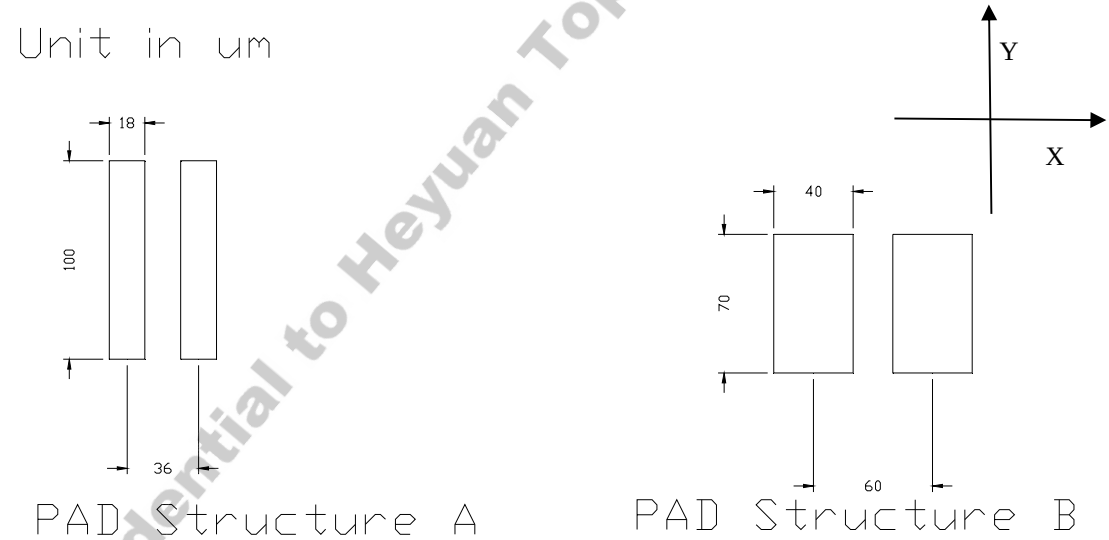


Figure 5-3 SSD1655Z – Gold bump pads



Die Size (after sawing)	13130 ± 50um x 1140 ± 50um
Die Thickness	300 ± 25um
Typical bump height	12um

Table 5-1: SSD1655 pad coordinates

Pad number	Pin Name	X	Y	Pad number	Pin Name	X	Y
1	DUMMY	-6390	-505	72	PVSS	-2130	-505
2	DUMMY	-6330	-505	73	PVSS	-2070	-505
3	GDR	-6270	-505	74	PVSS	-2010	-505
4	GDR	-6210	-505	75	PVSS	-1950	-505
5	GDR	-6150	-505	76	PVSS	-1890	-505
6	GDR	-6090	-505	77	PVSS	-1830	-505
7	GDR	-6030	-505	78	PVSS	-1770	-505
8	GDR	-5970	-505	79	PVSS	-1710	-505
9	GDR	-5910	-505	80	PVSS	-1650	-505
10	GDR	-5850	-505	81	PVSS	-1590	-505
11	VSS	-5790	-505	82	PVSS	-1530	-505
12	RESE	-5730	-505	83	PVSS	-1470	-505
13	RESE	-5670	-505	84	PVSS	-1410	-505
14	VSS	-5610	-505	85	PVSS	-1350	-505
15	FB1	-5550	-505	86	PVSS	-1290	-505
16	FB1	-5490	-505	87	PVSS	-1230	-505
17	FB2	-5430	-505	88	PVSS	-1170	-505
18	FB2	-5370	-505	89	VSS	-1110	-505
19	VSS	-5310	-505	90	VSS	-1050	-505
20	VH	-5250	-505	91	VSS	-990	-505
21	VH	-5190	-505	92	VSS	-930	-505
22	VH	-5130	-505	93	VSS	-870	-505
23	VH	-5070	-505	94	VSS	-810	-505
24	VH	-5010	-505	95	VSS	-750	-505
25	VH	-4950	-505	96	VSS	-690	-505
26	VH	-4890	-505	97	AVSS	-630	-505
27	V0	-4830	-505	98	AVSS	-570	-505
28	V0	-4770	-505	99	AVSS	-510	-505
29	V0	-4710	-505	100	AVSS	-450	-505
30	V0	-4650	-505	101	AVSS	-390	-505
31	V0	-4590	-505	102	VSSBG	-330	-505
32	V0	-4530	-505	103	VSSBG	-270	-505
33	V0	-4470	-505	104	VSSBG	-210	-505
34	V1	-4410	-505	105	VSSBG	-150	-505
35	V1	-4350	-505	106	VSSBG	-90	-505
36	V1	-4290	-505	107	VSS	-30	-505
37	V1	-4230	-505	108	VPP	30	-505
38	V1	-4170	-505	109	VPP	90	-505
39	V1	-4110	-505	110	VPP	150	-505
40	V2	-4050	-505	111	VPP	210	-505
41	V2	-3990	-505	112	VPP	270	-505
42	V2	-3930	-505	113	VPP	330	-505
43	V2	-3870	-505	114	VPP	390	-505
44	V2	-3810	-505	115	VPP	450	-505
45	V2	-3750	-505	116	VPP	510	-505
46	V3	-3690	-505	117	VPP	570	-505
47	V3	-3630	-505	118	VPP	630	-505
48	V3	-3570	-505	119	VPP	690	-505
49	V3	-3510	-505	120	VPP	750	-505
50	V3	-3450	-505	121	VPP	810	-505
51	V3	-3390	-505	122	VPP	870	-505
52	V4	-3330	-505	123	CL	930	-505
53	V4	-3270	-505	124	CL	990	-505
54	V4	-3210	-505	125	VSS	1050	-505
55	V4	-3150	-505	126	CLS	1110	-505
56	V4	-3090	-505	127	CLS	1170	-505
57	V4	-3030	-505	128	VDDIO	1230	-505
58	VDD	-2970	-505	129	SI	1290	-505
59	VDD	-2910	-505	130	SI	1350	-505
60	VDD	-2850	-505	131	SO	1410	-505
61	VDD	-2790	-505	132	SO	1470	-505
62	VDD	-2730	-505	133	SCLK	1530	-505
63	VDD	-2670	-505	134	SCLK	1590	-505
64	VDD	-2610	-505	135	CSB	1650	-505
65	VDD	-2550	-505	136	CSB	1710	-505
66	TPA	-2490	-505	137	RESB	1770	-505
67	TPB	-2430	-505	138	RESB	1830	-505
68	TPC	-2370	-505	139	ACK	1890	-505
69	PVSS	-2310	-505	140	ACK	1950	-505
70	PVSS	-2250	-505	141	IDLE/SLEEP	2010	-505
71	PVSS	-2190	-505	142	IDLE/SLEEP	2070	-505

Pad number	Pin Name	X	Y		Pad number	Pin Name	X	Y
143	VSS	2130	-505		215	DUMMY	6282	490
144	EXT_VDD	2190	-505		216	SEG 239	6246	490
145	EXT_VDD	2250	-505		217	SEG 237	6210	490
146	VDDIO	2310	-505		218	SEG 235	6174	490
147	VDDIO	2370	-505		219	SEG 233	6138	490
148	VDDIO	2430	-505		220	SEG 231	6102	490
149	VDDIO	2490	-505		221	SEG 229	6066	490
150	VDDIO	2550	-505		222	SEG 227	6030	490
151	VDDIO	2610	-505		223	SEG 225	5994	490
152	VCIBG	2670	-505		224	SEG 223	5958	490
153	VCIBG	2730	-505		225	SEG 221	5922	490
154	VCIBG	2790	-505		226	SEG 219	5886	490
155	AVCI	2850	-505		227	SEG 217	5850	490
156	AVCI	2910	-505		228	SEG 215	5814	490
157	AVCI	2970	-505		229	SEG 213	5778	490
158	VCI	3030	-505		230	SEG 211	5742	490
159	VCI	3090	-505		231	SEG 209	5706	490
160	VCI	3150	-505		232	SEG 207	5670	490
161	VCI	3210	-505		233	SEG 205	5634	490
162	VCI	3270	-505		234	SEG 203	5598	490
163	VCI	3330	-505		235	SEG 201	5562	490
164	VCI	3390	-505		236	SEG 199	5526	490
165	VCI	3450	-505		237	SEG 197	5490	490
166	VCI	3510	-505		238	SEG 195	5454	490
167	VCI	3570	-505		239	SEG 193	5418	490
168	VCIX2G	3630	-505		240	SEG 191	5382	490
169	VCIX2G	3690	-505		241	SEG 189	5346	490
170	VCIX2G	3750	-505		242	SEG 187	5310	490
171	VCIX2G	3810	-505		243	SEG 185	5274	490
172	VCIX2G	3870	-505		244	SEG 183	5238	490
173	VCIX2	3930	-505		245	SEG 181	5202	490
174	VCIX2	3990	-505		246	SEG 179	5166	490
175	VCIX2	4050	-505		247	SEG 177	5130	490
176	VCIX2	4110	-505		248	SEG 175	5094	490
177	VCIX2	4170	-505		249	SEG 173	5058	490
178	VREG	4230	-505		250	SEG 171	5022	490
179	VREG	4290	-505		251	SEG 169	4986	490
180	VREG	4350	-505		252	SEG 167	4950	490
181	VREG	4410	-505		253	SEG 165	4914	490
182	VREG	4470	-505		254	SEG 163	4878	490
183	VREG	4530	-505		255	SEG 161	4842	490
184	VREG	4590	-505		256	SEG 159	4806	490
185	VREG	4650	-505		257	SEG 157	4770	490
186	VREG	4710	-505		258	SEG 155	4734	490
187	VSS	4770	-505		259	SEG 153	4698	490
188	VREF	4830	-505		260	SEG 151	4662	490
189	VREF	4890	-505		261	SEG 149	4626	490
190	VEXT	4950	-505		262	SEG 147	4590	490
191	VEXT	5010	-505		263	SEG 145	4554	490
192	VEXT_1P25	5070	-505		264	SEG 143	4518	490
193	VSS	5130	-505		265	SEG 141	4482	490
194	C1P	5190	-505		266	SEG 139	4446	490
195	C1P	5250	-505		267	SEG 137	4410	490
196	C1P	5310	-505		268	SEG 135	4374	490
197	C1P	5370	-505		269	SEG 133	4338	490
198	C1P	5430	-505		270	SEG 131	4302	490
199	C1P	5490	-505		271	SEG 129	4266	490
200	C1P	5550	-505		272	SEG 127	4230	490
201	C1P	5610	-505		273	SEG 125	4194	490
202	C1P	5670	-505		274	SEG 123	4158	490
203	C1P	5730	-505		275	SEG 121	4122	490
204	C1N	5790	-505		276	SEG 119	4086	490
205	C1N	5850	-505		277	SEG 117	4050	490
206	C1N	5910	-505		278	SEG 115	4014	490
207	C1N	5970	-505		279	SEG 113	3978	490
208	C1N	6030	-505		280	SEG 111	3942	490
209	C1N	6090	-505		281	SEG 109	3906	490
210	C1N	6150	-505		282	SEG 107	3870	490
211	C1N	6210	-505		283	SEG 105	3834	490
212	C1N	6270	-505		284	SEG 103	3798	490
213	C1N	6330	-505		285	SEG 101	3762	490
214	DUMMY	6390	-505		286	SEG 99	3726	490

Pad number	Pin Name	X	Y
287	SEG 97	3690	490
288	SEG 95	3654	490
289	SEG 93	3618	490
290	SEG 91	3582	490
291	SEG 89	3546	490
292	SEG 87	3510	490
293	SEG 85	3474	490
294	SEG 83	3438	490
295	SEG 81	3402	490
296	SEG 79	3366	490
297	SEG 77	3330	490
298	SEG 75	3294	490
299	SEG 73	3258	490
300	SEG 71	3222	490
301	SEG 69	3186	490
302	SEG 67	3150	490
303	SEG 65	3114	490
304	SEG 63	3078	490
305	SEG 61	3042	490
306	SEG 59	3006	490
307	SEG 57	2970	490
308	SEG 55	2934	490
309	SEG 53	2898	490
310	SEG 51	2862	490
311	SEG 49	2826	490
312	SEG 47	2790	490
313	SEG 45	2754	490
314	SEG 43	2718	490
315	SEG 41	2682	490
316	SEG 39	2646	490
317	SEG 37	2610	490
318	SEG 35	2574	490
319	SEG 33	2538	490
320	SEG 31	2502	490
321	SEG 29	2466	490
322	SEG 27	2430	490
323	SEG 25	2394	490
324	SEG 23	2358	490
325	SEG 21	2322	490
326	SEG 19	2286	490
327	SEG 17	2250	490
328	SEG 15	2214	490
329	SEG 13	2178	490
330	SEG 11	2142	490
331	SEG 9	2106	490
332	SEG 7	2070	490
333	SEG 5	2034	490
334	SEG 3	1998	490
335	SEG 1	1962	490
336	DUMMY	1926	490
337	DUMMY	1890	490
338	DUMMY	1854	490
339	DUMMY	1818	490
340	DUMMY	1782	490
341	DUMMY	1746	490
342	COM 95	1710	490
343	COM 94	1674	490
344	COM 93	1638	490
345	COM 92	1602	490
346	COM 91	1566	490
347	COM 90	1530	490
348	COM 89	1494	490
349	COM 88	1458	490
350	COM 87	1422	490
351	COM 86	1386	490
352	COM 85	1350	490
353	COM 84	1314	490
354	COM 83	1278	490
355	COM 82	1242	490
356	COM 81	1206	490
357	COM 80	1170	490
358	COM 79	1134	490

Pad number	Pin Name	X	Y
359	COM 78	1098	490
360	COM 77	1062	490
361	COM 76	1026	490
362	COM 75	990	490
363	COM 74	954	490
364	COM 73	918	490
365	COM 72	882	490
366	COM 71	846	490
367	COM 70	810	490
368	COM 69	774	490
369	COM 68	738	490
370	COM 67	702	490
371	COM 66	666	490
372	COM 65	630	490
373	COM 64	594	490
374	COM 63	558	490
375	COM 62	522	490
376	COM 61	486	490
377	COM 60	450	490
378	COM 59	414	490
379	COM 58	378	490
380	COM 57	342	490
381	COM 56	306	490
382	COM 55	270	490
383	COM 54	234	490
384	COM 53	198	490
385	COM 52	162	490
386	COM 51	126	490
387	COM 50	90	490
388	COM 49	54	490
389	COM 48	18	490
390	COM 47	-18	490
391	COM 46	-54	490
392	COM 45	-90	490
393	COM 44	-126	490
394	COM 43	-162	490
395	COM 42	-198	490
396	COM 41	-234	490
397	COM 40	-270	490
398	COM 39	-306	490
399	COM 38	-342	490
400	COM 37	-378	490
401	COM 36	-414	490
402	COM 35	-450	490
403	COM 34	-486	490
404	COM 33	-522	490
405	COM 32	-558	490
406	COM 31	-594	490
407	COM 30	-630	490
408	COM 29	-666	490
409	COM 28	-702	490
410	COM 27	-738	490
411	COM 26	-774	490
412	COM 25	-810	490
413	COM 24	-846	490
414	COM 23	-882	490
415	COM 22	-918	490
416	COM 21	-954	490
417	COM 20	-990	490
418	COM 19	-1026	490
419	COM 18	-1062	490
420	COM 17	-1098	490
421	COM 16	-1134	490
422	COM 15	-1170	490
423	COM 14	-1206	490
424	COM 13	-1242	490
425	COM 12	-1278	490
426	COM 11	-1314	490
427	COM 10	-1350	490
428	COM 9	-1386	490
429	COM 8	-1422	490
430	COM 7	-1458	490

Pad number	Pin Name	X	Y
431	COM 6	-1494	490
432	COM 5	-1530	490
433	COM 4	-1566	490
434	COM 3	-1602	490
435	COM 2	-1638	490
436	COM 1	-1674	490
437	COM 0	-1710	490
438	DUMMY	-1746	490
439	DUMMY	-1782	490
440	DUMMY	-1818	490
441	DUMMY	-1854	490
442	DUMMY	-1890	490
443	DUMMY	-1926	490
444	SEG 0	-1962	490
445	SEG 2	-1998	490
446	SEG 4	-2034	490
447	SEG 6	-2070	490
448	SEG 8	-2106	490
449	SEG 10	-2142	490
450	SEG 12	-2178	490
451	SEG 14	-2214	490
452	SEG 16	-2250	490
453	SEG 18	-2286	490
454	SEG 20	-2322	490
455	SEG 22	-2358	490
456	SEG 24	-2394	490
457	SEG 26	-2430	490
458	SEG 28	-2466	490
459	SEG 30	-2502	490
460	SEG 32	-2538	490
461	SEG 34	-2574	490
462	SEG 36	-2610	490
463	SEG 38	-2646	490
464	SEG 40	-2682	490
465	SEG 42	-2718	490
466	SEG 44	-2754	490
467	SEG 46	-2790	490
468	SEG 48	-2826	490
469	SEG 50	-2862	490
470	SEG 52	-2898	490
471	SEG 54	-2934	490
472	SEG 56	-2970	490
473	SEG 58	-3006	490
474	SEG 60	-3042	490
475	SEG 62	-3078	490
476	SEG 64	-3114	490
477	SEG 66	-3150	490
478	SEG 68	-3186	490
479	SEG 70	-3222	490
480	SEG 72	-3258	490
481	SEG 74	-3294	490
482	SEG 76	-3330	490
483	SEG 78	-3366	490
484	SEG 80	-3402	490
485	SEG 82	-3438	490
486	SEG 84	-3474	490
487	SEG 86	-3510	490
488	SEG 88	-3546	490
489	SEG 90	-3582	490
490	SEG 92	-3618	490
491	SEG 94	-3654	490
492	SEG 96	-3690	490
493	SEG 98	-3726	490
494	SEG 100	-3762	490
495	SEG 102	-3798	490
496	SEG 104	-3834	490
497	SEG 106	-3870	490
498	SEG 108	-3906	490
499	SEG 110	-3942	490
500	SEG 112	-3978	490
501	SEG 114	-4014	490
502	SEG 116	-4050	490

Pad number	Pin Name	X	Y
503	SEG 118	-4086	490
504	SEG 120	-4122	490
505	SEG 122	-4158	490
506	SEG 124	-4194	490
507	SEG 126	-4230	490
508	SEG 128	-4266	490
509	SEG 130	-4302	490
510	SEG 132	-4338	490
511	SEG 134	-4374	490
512	SEG 136	-4410	490
513	SEG 138	-4446	490
514	SEG 140	-4482	490
515	SEG 142	-4518	490
516	SEG 144	-4554	490
517	SEG 146	-4590	490
518	SEG 148	-4626	490
519	SEG 150	-4662	490
520	SEG 152	-4698	490
521	SEG 154	-4734	490
522	SEG 156	-4770	490
523	SEG 158	-4806	490
524	SEG 160	-4842	490
525	SEG 162	-4878	490
526	SEG 164	-4914	490
527	SEG 166	-4950	490
528	SEG 168	-4986	490
529	SEG 170	-5022	490
530	SEG 172	-5058	490
531	SEG 174	-5094	490
532	SEG 176	-5130	490
533	SEG 178	-5166	490
534	SEG 180	-5202	490
535	SEG 182	-5238	490
536	SEG 184	-5274	490
537	SEG 186	-5310	490
538	SEG 188	-5346	490
539	SEG 190	-5382	490
540	SEG 192	-5418	490
541	SEG 194	-5454	490
542	SEG 196	-5490	490
543	SEG 198	-5526	490
544	SEG 200	-5562	490
545	SEG 202	-5598	490
546	SEG 204	-5634	490
547	SEG 206	-5670	490
548	SEG 208	-5706	490
549	SEG 210	-5742	490
550	SEG 212	-5778	490
551	SEG 214	-5814	490
552	SEG 216	-5850	490
553	SEG 218	-5886	490
554	SEG 220	-5922	490
555	SEG 222	-5958	490
556	SEG 224	-5994	490
557	SEG 226	-6030	490
558	SEG 228	-6066	490
559	SEG 230	-6102	490
560	SEG 232	-6138	490
561	SEG 234	-6174	490
562	SEG 236	-6210	490
563	SEG 238	-6246	490
564	DUMMY	-6282	490

6 PIN DESCRIPTIONS

Key:

I = Input	O =Output
IO = Bi-directional (input/output)	P = Power pin

Pin Name	Pin Type	Description
V_{DD}	P	This is the VDD regulator output pin. It also serves as the power supply of the logic block. A capacitor is required to connect to this pin.
V_{DDIO}	P	This is the MCU interface logic level.
V_{CI}	P	Power supply for analog part of the chip.
AVCI	P	VCI for analog
VCIBG	P	VCI for reference
V_{SS}	P	This is a ground pin
AVss	P	Ground for analog
VSSBG	P	Ground for reference
PVss	P	Ground for SEG cell, booster gate driver and V1-V4 buffers
VPP	P	Power pin for LUT OTP programming
VREG	O	A regulated output voltage for internal analog circuit
V_0	P	It is the high voltage power input pin and panel driving voltage. The voltage level is programmable by command.
V_1	O	Panel driving voltage. When bias divider is enabled with the presence of V0, the voltage is equal to V0 – V4.
V_2	O	Panel driving voltage. When bias divider is enabled with the presence of V0, the voltage is equal to V0 – 2*V4
V_3	O	Panel driving voltage. When bias divider is enabled with the presence of V0, the voltage is equal to 2*V4.
V_4	O	Low non-zero bias voltage for panel driving. The voltage level can be programmable by command.
CL	IO	This pin is the display clock input/output.
CLS	I	This pin is the internal clock enable pin. When this pin is pulled high to V_{DDIO}, internal clock is enabled. The internal clock will be disabled when it is pulled low to VSS, an external clock source must be input to CL pin for normal operation.
SI	I	SPI data input to IC
SO	O	SPI data output from IC
SCLK	I	SPI clock signal
CS#	I	These pins are the chip select inputs for communication between MCU. To select the chip CS# must be low.

Pin Name	Pin Type	Description
RES#	I	This pin is the reset signal input. Initialization of the chip is started once this pin is pulled low. Minimum pulse width for reset sequence is 20us. If RES# is asserted while the driver IC is in SLEEP mode, no ACK signal will be returned. The RESET operation will however be carried out and the driver IC will not leave SLEEP mode. At DEEPSLEEP mode, this pin should keep high for minimum power consumption.
ACK	O	This is an output pin indicating the status of the chip in the following way. Output H continously: Indicates the chip is in wake up state Output L continously: Indicates the chip is in SLEEP mode A L pulse for 2us: Indicates command operation is completed Commands which will generate the L pulse include UPDATE, BATTLEVEL, HW RESET, OTPWRITE, OTPREAD, ABORT The falling-edge of the ACK signal indicates that a command operation is complete, it is not necessary to wait for the rising-edge of ACK before sending the next command. If commands are sent while the driver IC is busy and before the ACK pulse has been generated then completion of these commands is not guaranteed.
IDLE/SLEEP	I	When this pin is at low level, the driver IC will enter Sleep mode. RAM content and register will be retained in this mode. When this pin is at high level, the driver IC will resume to IDLE mode.
EXT_VDD	I	A L input at this pin indicate the use of internal VDD regulator. This pin must be connected to VSS for normal operation
COM0 ~ COM95	O	These pins provide the Common driving signals to the Bistable panel.
SEG0 ~ SEG239	O	These pins provide the Segment driving signals to the Bistable panel.
C1N, C1P	IO	Charge Pump flying capacitor terminal. Connect a capacitor between C1N and C1P.
VCIX2	P	Connect to VCIX2G for normal operation
VCIX2G	O	Charge Pump output voltage. Connect with a capacitor to V_{SS}.
FB1	I	Feedback pin for booster controller
FB2	I	Feedback pin for booster controller
GDR	O	Gate drive signal for booster
VH	P	High voltage power pin. Connect booster output to this pin for V0 to V4 generations.
RESE	I	Current sense input for booster circuit
VREF	I	Testing reserved pins
VEXT	I	Testing reserved pins

Pin Name	Pin Type	Description
VEXT_1P25	I/O	Testing reserved pins
TPA	I/O	Testing reserved pins
TPB	I/O	Testing reserved pins
TPC	I/O	Testing reserved pins
DUMMY	-	Dummy Bump pads No circuit is connected underneath

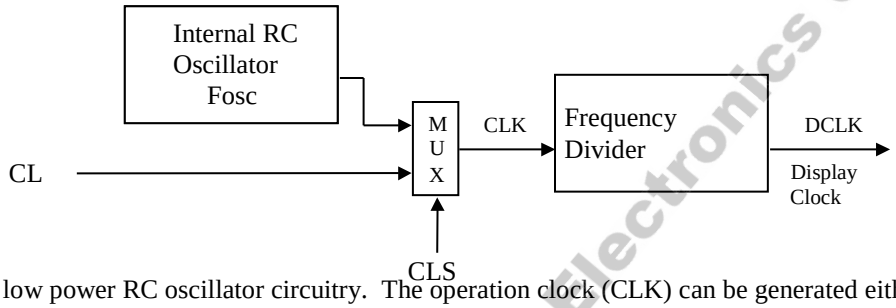
7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 Reset Circuit

When RES# input is LOW, the chip is initialized to the POR status.

7.2 Oscillator Circuit and Display Time Generator

Figure 7-1 : Oscillator Circuit and Display Time Generator



This module is an on-chip low power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be left open. Pulling CLS pin low disables internal oscillator and external clock must be connected to CL pins for proper operation.

7.3 Command Decoder and MCU Interface

This module determines if the input data will be interpreted as data, or a command.

7.4 MCU Serial Interface

SSD1655 is configured via a simple 4-wire SPI compatible interface (SI, SO, SCLK and CS#) as slave. This interface is also used to read and write buffered data.
Transfers on the SPI interface are Little Endian, that is, a succession of Bytes is transferred Least-Significant-Byte first. In each Byte, the Most-Significant-Bit is transferred first.

All transactions on the SPI interface start with a header byte containing a R/W bit, and a 6-bit address (A5 – A0). The CS# pin must be kept low during transfers on the SPI bus. If CS# goes high during the transfer of a header byte or during read/write from/to a register, the transfer will be cancelled.

Refer to section 13 for SPI timing details and diagrams.

7.5 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The GDDRAM can be accessed through SPI interface.

Below diagrams illustrate the mapping between memory and the output SEG/COM under different NUMROWS, NUMCOLS, and IMGORIENT setting

Figure 7-2 : Mapping illustration when all COM and SEG are used

NUMROWS 96d
NUMCOLS 240d
IMGORIENT 00b

		SEG0 - SEG7	SEG8 - SEG15	SEG16 - SEG23	...	SEG208 - SEG215	SEG216 - SEG223	SEG224 - SEG231	SEG232 - SEG239	Output channels
		0	8	16		208	216	224	232	Column addr
COM0	0	D0[7:0]	D1[7:0]					D28[7:0]	D29[7:0]	
COM1	1									
COM2	2									
...										
COM92	92									
COM93	93									
COM94	94									
COM95	95	D2850[7:0]	D2851[7:0]					D2878[7:0]	D2879[7:0]	
Output channels	Row addr									

NUMROWS 96d
NUMCOLS 240d
IMGORIENT 01b

		SEG0 - SEG7	SEG8 - SEG15	SEG16 - SEG23	...	SEG208 - SEG215	SEG216 - SEG223	SEG224 - SEG231	SEG232 - SEG239	Output channels
		0	8	16		208	216	224	232	Column addr
COM0	95	D2850[7:0]	D2851[7:0]					D2878[7:0]	D2879[7:0]	
COM1	94									
COM2	93									
...										
COM92	3									
COM93	2									
COM94	1									
COM95	0	D0[7:0]	D1[7:0]					D28[7:0]	D29[7:0]	
Output channels	Row addr									

NUMROWS 96d
NUMCOLS 240d
IMGORIENT 10b

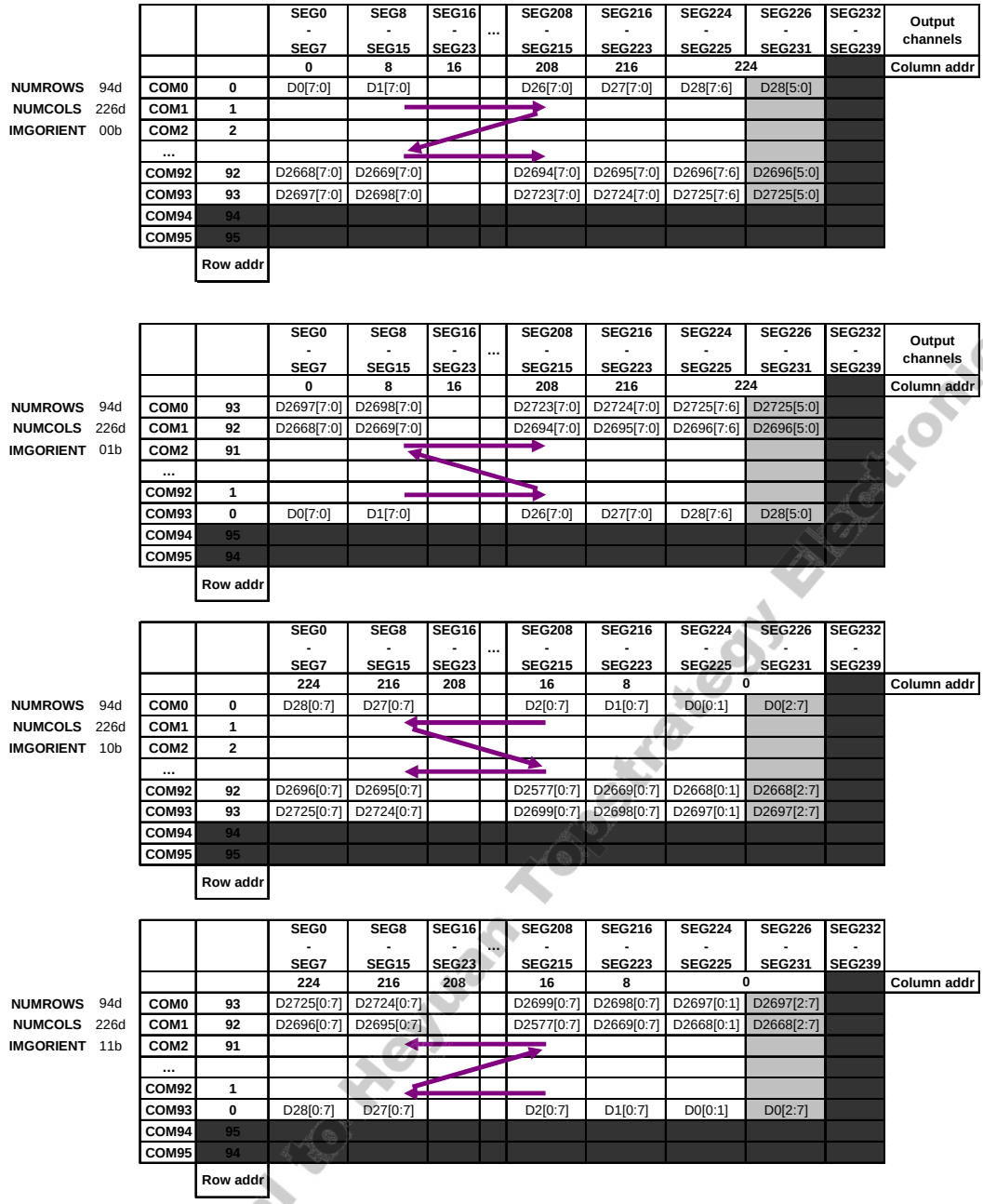
		SEG0 - SEG7	SEG8 - SEG15	SEG16 - SEG23	...	SEG208 - SEG215	SEG216 - SEG223	SEG224 - SEG231	SEG232 - SEG239	Output channels
		232	224	216		24	16	8	0	Column addr
COM0	0	D29[0:7]	D28[0:7]					D1[0:7]	D0[0:7]	
COM1	1									
COM2	2									
...										
COM92	92									
COM93	93									
COM94	94									
COM95	95	D2879[0:7]	D2878[0:7]					D2851[0:7]	D2850[0:7]	
Output channels	Row addr									

NUMROWS 96d
NUMCOLS 240d
IMGORIENT 11b

		SEG0 - SEG7	SEG8 - SEG15	SEG16 - SEG23	...	SEG208 - SEG215	SEG216 - SEG223	SEG224 - SEG231	SEG232 - SEG239	Output channels
		232	224	216		24	16	8	0	Column addr
COM0	95	D2879[0:7]	D2878[0:7]					D2851[0:7]	D2850[0:7]	
COM1	94									
COM2	93									
...										
COM92	3									
COM93	2									
COM94	1									
COM95	0	D29[0:7]	D28[0:7]					D1[0:7]	D0[0:7]	
Output channels	Row addr									

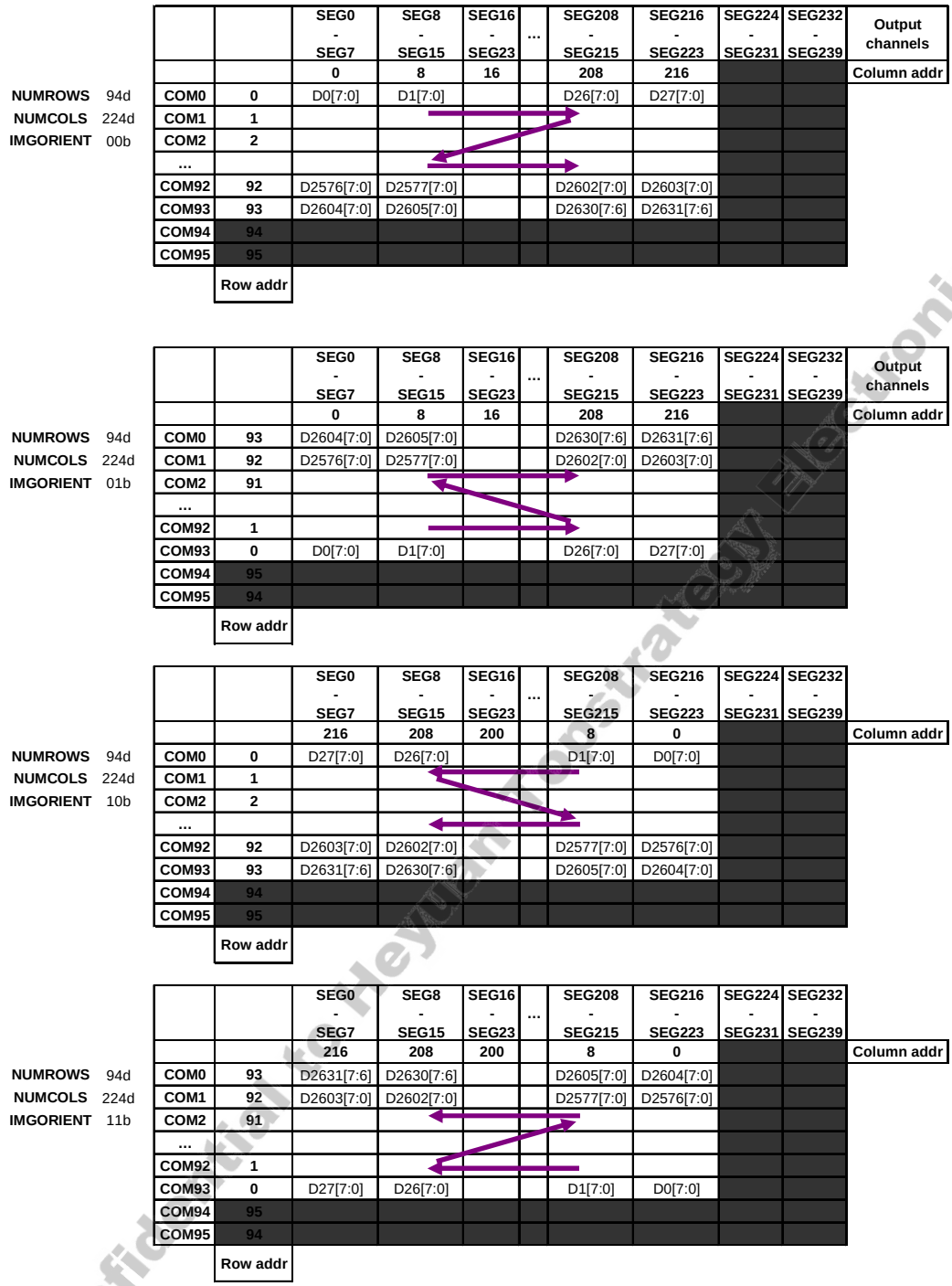
COM0, SEG0 is D0 bit 7 when IMGORIENT = 00b
COM0, SEG0 is D2879 bit 0 when IMGORIENT = 11b

Figure 7-3 : Mapping illustration under partial COM and partial SEG case (non-multiple of 8 columns)



COM0, SEG0 is D0 bit 7 when IMGORIENT = 00b
COM0, SEG0 is D2725 bit 0 when IMGORIENT = 11b

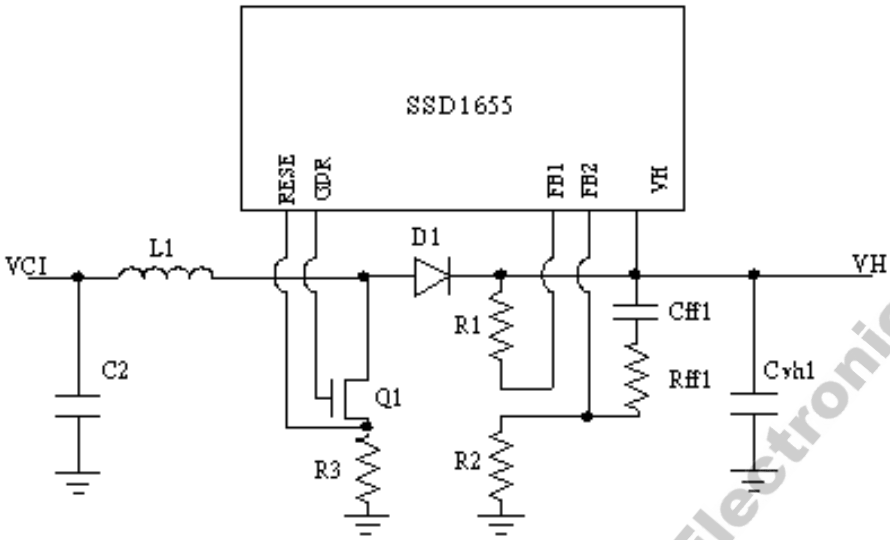
Figure 7-4 : Mapping illustration under partial COM and partial SEG case (multiple of 8 columns)



COM0, SEG0 is D0 bit 7 when IMGORIENT = 00b
COM0, SEG0 is D2631 bit 0 when IMGORIENT = 11b

7.6 Booster controller

This is an inductor type booster controller. External components such as inductor, diode, power MOSFET, capacitors are required for operations and the output is regulated at programmable voltage.



- Booster is designed to optimize with 2.3 to 2.6V VCI range.

7.7 Bias Voltage Generator

This module generates the high voltage required for display driving output. It takes a single supply input and generates necessary bias voltage. It consists of:

1. Bias Divider
2. Bias Voltage Buffer

The intermediate voltages V1, V2 and V3 are derived from V0 and V4 as shown below.

Table 7-1: Value of bias voltages

Bias voltage	Value
V0	Highest bias voltage in system
V1	V0 – V4
V2	V0 – 2 * V4
V3	2 * V4
V4	Lowest non-zero bias voltage set by command
V5	Vss

V0 can be set from 8.25 to 40V in steps of 0.25V
V4 can be set from 0V (First field data Disable), 2.25 to 10V in steps of 0.25V
This block is powered by VH.

7.8 Display Timing control

When there is update of the display, the control unit reads the temperature value to set the appropriate driving voltages, timings and waveform. The setting values are either based on the LUT setting of the corresponding temperature in the OTP, or user can use register values control the voltages and timings. The bias voltage generator is programmed to provide the correct voltages to support the display update.

7.9 Segment Drivers / Common Drivers

The Segment/Common Driver Circuits works as a level shifter, which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal clock, which comes from the Display Timing Control. The voltage levels are given by the voltage bias generator.

7.10 VDD regulator

With power supplied from VCI, this block provides a regulated output voltage VDD for logic operations. A capacitor is required at VDD level.

7.11 OTP and Waveform setting

The driver IC contains OTP with total size of 4K bits for storing

- LUT parameters, which are used to control voltage and timings of display waveform
- Configuration constants, which are used to indicate the panel configurations
- Production setting, which are used to store necessary production and testing data

The default state of the OTP memory (before programming) is all ones.

7.11.1 Waveform and Temperature LUT

The LUT of SSD1655 consists of Indirect LUT and Direct LUT portion.

The indirect LUT stores the mapping between temperatures register index to Direct LUT index. It has 256 entries. The mapping of temperature register index to temperature will depend on the temperature sensor in use.

The direct LUT stores the timing and voltage information. Each LUT index corresponds to one set of timing and voltage information. Altogether there are 60 direct LUT indices.

7.11.1.1 Illustration of Indirect LUT

Table 7-2: Example Mapping of Temperature register index to LUT index

Temperature register Index	LUT Index ilutn[5:0]
00000000	0
00000001	0
00000010	0
00000011	0
00000100	1
. . .	. . .
11111100	35
11111101	36
11111110	…
11111111	38

7.11.1.2 Illustration of Direct LUT

Table 7-3: Example Illustration on the Direct LUT content

LUT Index (6 bits)	VlcdBlank (V)	VlcdWrite (V)	SlotBlank (us)	SlotWrite (us)	Vd (V)
0	30	30	10000	5000	7
1	30	30	10000	4500	6.5
2	28	26	8000	4000	6
…					
14	26	24	3000	2000	5
15	25.5	24	2800	1900	4.8
16	25.0	24	2600	1800	4.6
…					
59	15	14	500	250	3

The above table shows actual values instead of digital values as defined.

Table 7-4: Parameters of each temperature entry in OTP

Variable	Description	Maximum setting	Minimum setting	Step size	Number of steps	bits	Operation Restriction
τ_w (µs)	Write time (slot width in Field 2)	51200	100	100	512	9	
Vs+Vd (V)	Vlcd Write Voltage (V0 voltage in Field 2)	40	8.25	0.25	128	7	Max: 40V Min: 8.25V
τ_b (µs)	Blank time (slot width in Field 1)	51200	100	100	512	9	
Vb (V)	Blank Voltage (V0 voltage in Field 1)	40	9	1.0	32	5	Max: 40V Min: 9V
Vd (V)	Data Voltage (V4 voltage)	10	2.25	0.25	32	5	Vd <= 1/3 x Vb; and Vd <= 1/3 x (Vs+Vd)
	Dummy (or assigned to above parameters)					1	
					Total	**36**	

Table 7-5: Equations for direct LUT setting

- Vd voltage = {Decimal value of Vd[4:0] x 0.25 + 2.25 }V
- Vs+Vd voltage = {Decimal value of Vs+Vd[6:0] x 0.25 + 8.25 }V
- Vb voltage = {Decimal value of Vb[4:0] x 1 + 9 }V
- τb duration = {Decimal value of τb[8:0] x 100 + 100 }us
- τw duration = {Decimal value of τw[8:0] x 100 + 100 }us

Table 7-6: Layout of OTP memory for Direct LUT Table (dlut n)

	Byte	Bits	
Write Time	0	0 – 7	LSB of Write time
Write Time	1	0	MSB of Write time
Select Voltage	1	1 – 7	
Blank Time	2	0 – 7	LSB of Blank time
Blank Time	3	0	MSB of Blank Time
Blank Voltage	3	1 – 5	
Data Voltage	3	6 -7	LSB of Data Voltage
Data Voltage	4	0 – 2	MSB of Data Voltage
Dummy Bit	4	3	

Note: the above table defines how data is arranged when using the LUTOVERRIDE command.
When using the LUTOVERRIDE command, 40-bits of data must be transferred, in this case Byte-4 bits 4-7 are all dummy data.

7.11.2 Configuration constants

The OTP also stores the configuration parameters of driver IC such as number of rows and columns, start row, scan direction etc.

Table 7-7 - Constants to be programmed into Chip

Byte	Bit	Definition	
0	7 – 0	Number of rows See SPI register NUMROWS (0x01) for definition	8 bits
1	7 – 0	Number of columns See SPI register NUMCOLS (0x02) for definition	8 bits
2	7 – 0	Lower byte of LUTVERS	8 bits
3	7 – 0	Upper byte of LUTVERS	8 bits
4	7	Enable/Disable extra termination row at end of Field 1 & 2 See SPI register DUMMYROWS (0x11) for definition	1 bit
4	6	Enable/Disable first field data See SPI register DUMMYROWS (0x11) for definition	1 bit
4	5	Extra Line Address Time See SPI register DUMMYROWS (0x11) for definition	1 bit
4	4 – 0	Number of dummy rows to apply at start of Field 2 See SPI register DUMMYROWS (0x11) for definition	5 bits
5	7 - 6	Dummy	2 bits
5	5 - 0	Temperature calibration value (Reserved)	6 bits
6	7 - 6	Scan direction See IMGORIENT SPI command for definition of the bits	2 bits
6	5	Dummy	1 bits
6	4	M/FR Polarity See SPI Register MCONF (0x16) for definition	1 bit
6	3 – 0	Reserved	4 bits
		TOTAL	**56 bits**

Table 7-8 - Alternative Memory Map view of configuration constants

Byte	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	NUMROWS (c0) 0x01[7:0]							
1	NUMCOLS (c1) 0x02[7:0]							
2	LUTVERS[7:0] (c2) 0x07[7:0]							
3	LUTVERS[15:8] (c3) 0x07[15:8]							
4	TerminRow (c4) 0x11[7]	Field1 EN (c5) 0x11[6]	ExtraLine (c11) 0x11[5]	DUMMYROWS (c6) 0x11[4:0]				
5	Dummy		Temperature Calibration (c7) 0x17[5:0]					
6	IMGORIENT (c8) 0x03[1:0]		Dummy	MCONF (c9) 0x16[0]	Reseved			

In the above diagram the number below the description consists of the SPI Register number, followed by the relevant bit(s).
These values will be programmed when the LCM is tested and can be overridden by the use of the appropriate SPI commands.

7.11.3 Summary of OTP usage

Table 7-9: OTP Layout and usage

	Size / Entries	# of Entries	Start Byte	End Byte	Size
Indirect LUT	6	256	0	191	1536 bits (192 bytes)
Direct LUT	36	60	192	461	2160 bits (270 bytes)
Configuration Bits	56	1	462	468	56 bits (7 bytes)
Reserve for production	184	1	469	491	184 bits (23 bytes)
Reserved for special use	160	1	492	511	160 bits (20 bytes)
				Total	4096 bits

Table 7-10: OTP Layout – expanded view

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
otpaddr[0]	ilut1[1:0]		ilut0[5:0]						
otpaddr[1]	ilut2[3:0]				ilut1[5:2]				
otpaddr[2]	ilut3[5:0]						ilut2[5:4]		
otpaddr[3]	ilut5[1:0]		ilut4[5:0]						
otpaddr[4]	ilut6[3:0]				ilut5[5:2]				
otpaddr[5]	ilut7[5:0]						ilut6[5:4]		
.									indirect
.									
.									
otpaddr[189]	ilut253[1:0]		ilut252[5:0]						
otpaddr[190]	ilut254[3:0]				ilut253[5:2]				
otpaddr[191]	ilut255[5:0]						ilut254[5:4]		
otpaddr[192]	dlut0_a[7:0]								
otpaddr[193]	dlut0_b[7:0]								
otpaddr[194]	dlut0_c[7:0]								
otpaddr[195]	dlut0_d[7:0]								
otpaddr[196]	dlut1_a[3:0]				dlut0_e[3:0]				
otpaddr[197]	dlut1_b[3:0]				dlut1_a[7:4]				
otpaddr[198]	dlut1_c[3:0]				dlut1_b[7:4]				
otpaddr[199]	dlut1_d[3:0]				dlut1_c[7:4]				
otpaddr[200]	dlut1_e[3:0]				dlut1_d[7:4]				
.									direct
.									
.									
otpaddr[457]	dlut59_a[3:0]				dlut58_e[3:0]				
otpaddr[458]	dlut59_b[3:0]				dlut59_a[7:4]				
otpaddr[459]	dlut59_c[3:0]				dlut59_b[7:4]				
otpaddr[460]	dlut59_d[3:0]				dlut59_c[7:4]				
otpaddr[461]	dlut59_e[3:0]				dlut59_d[7:4]				
otpaddr[462]	c0								
otpaddr[463]	c1								
otpaddr[464]	c2								
otpaddr[465]	c3								
otpaddr[466]	c4	c5	c11	c6					configuration
otpaddr[467]			c7						
otpaddr[468]	c8			c9	c10				
otpaddr[469]	reserved for production								
otpaddr[470]	reserved for production								
otpaddr[471]	reserved for production								
otpaddr[472]	reserved for production								
otpaddr[473]	reserved for production								
otpaddr[474]	reserved for production								
otpaddr[475]	reserved for production								reserved
otpaddr[476]	reserved for production								
.	reserved for production								
.	reserved for production								
.	reserved for production								
.	reserved for production								
.	reserved for production								
.	reserved for production								
.	reserved for production								
.	reserved for production								
otpaddr[511]	reserved for production								

8 Illustration of driving waveform

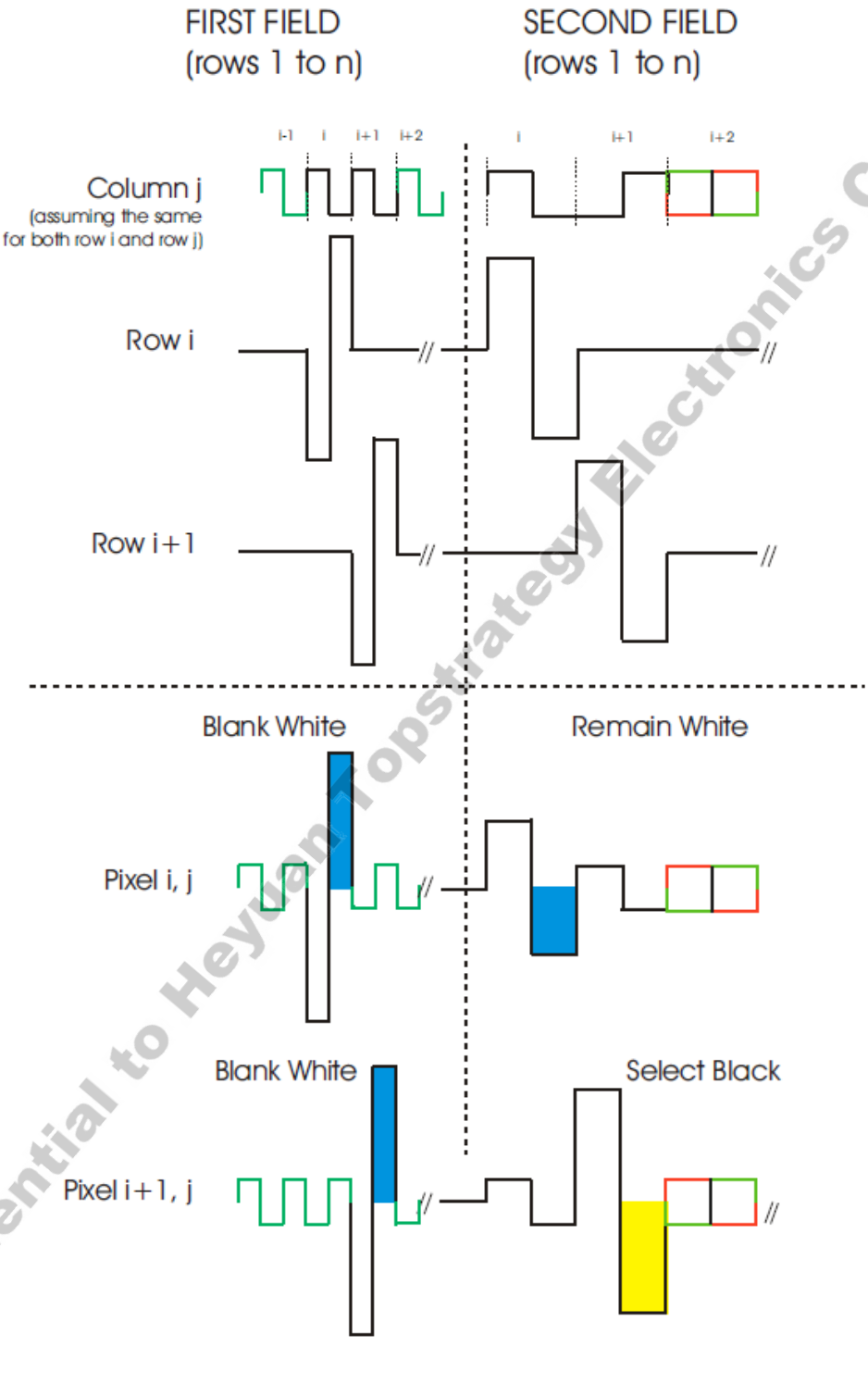


Figure 8-1: Schematic representation of a Two-field Addressing Scheme

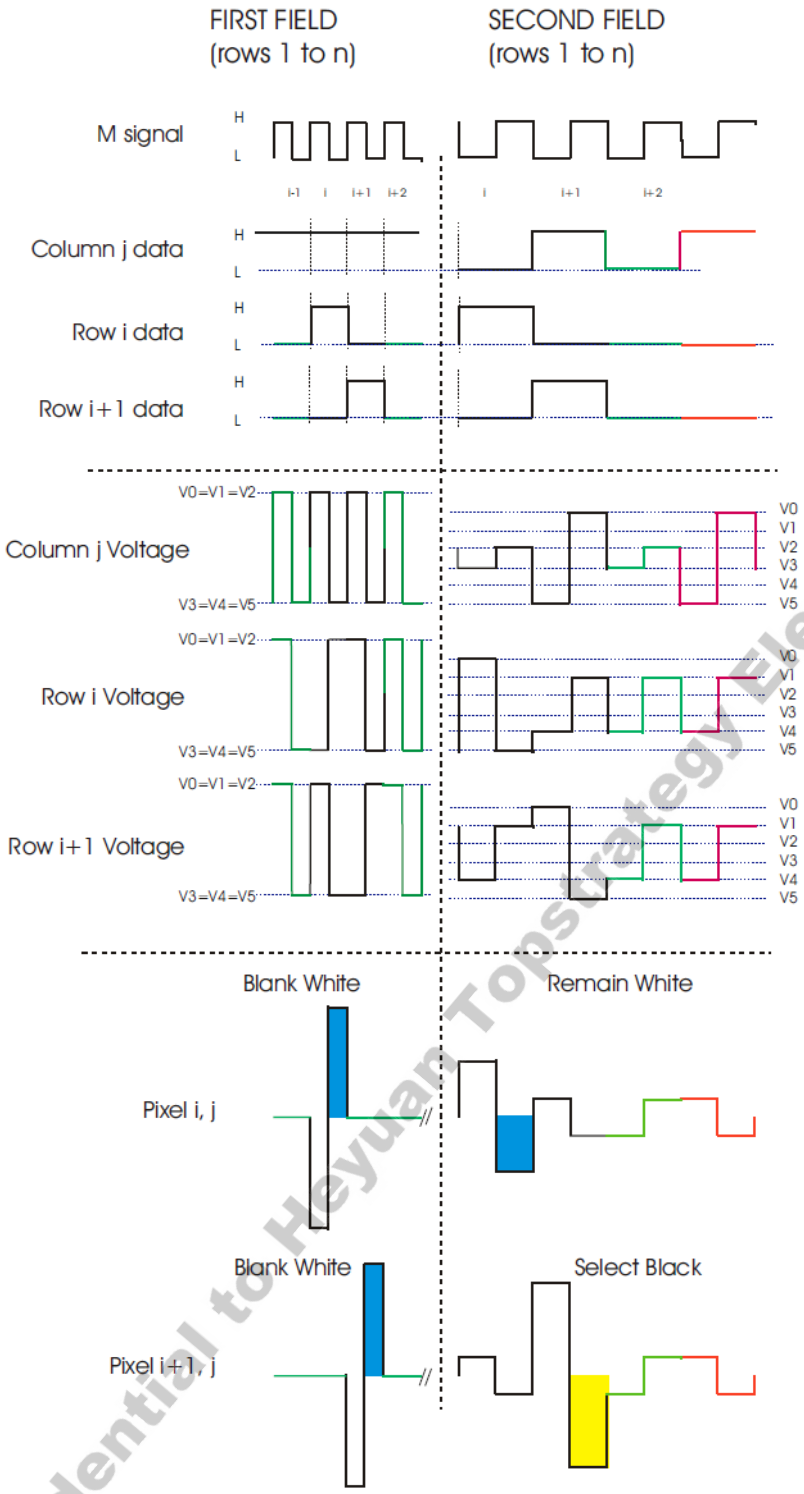


Figure 8-2: Illustration of how the required resultants of Figure 8-1 are generated.

Remark:

- Between First Field and Second Field, all SEG and all COM will be at Vss.
- Before First Field and Second Field, all SEG and all COM will be at Vss.

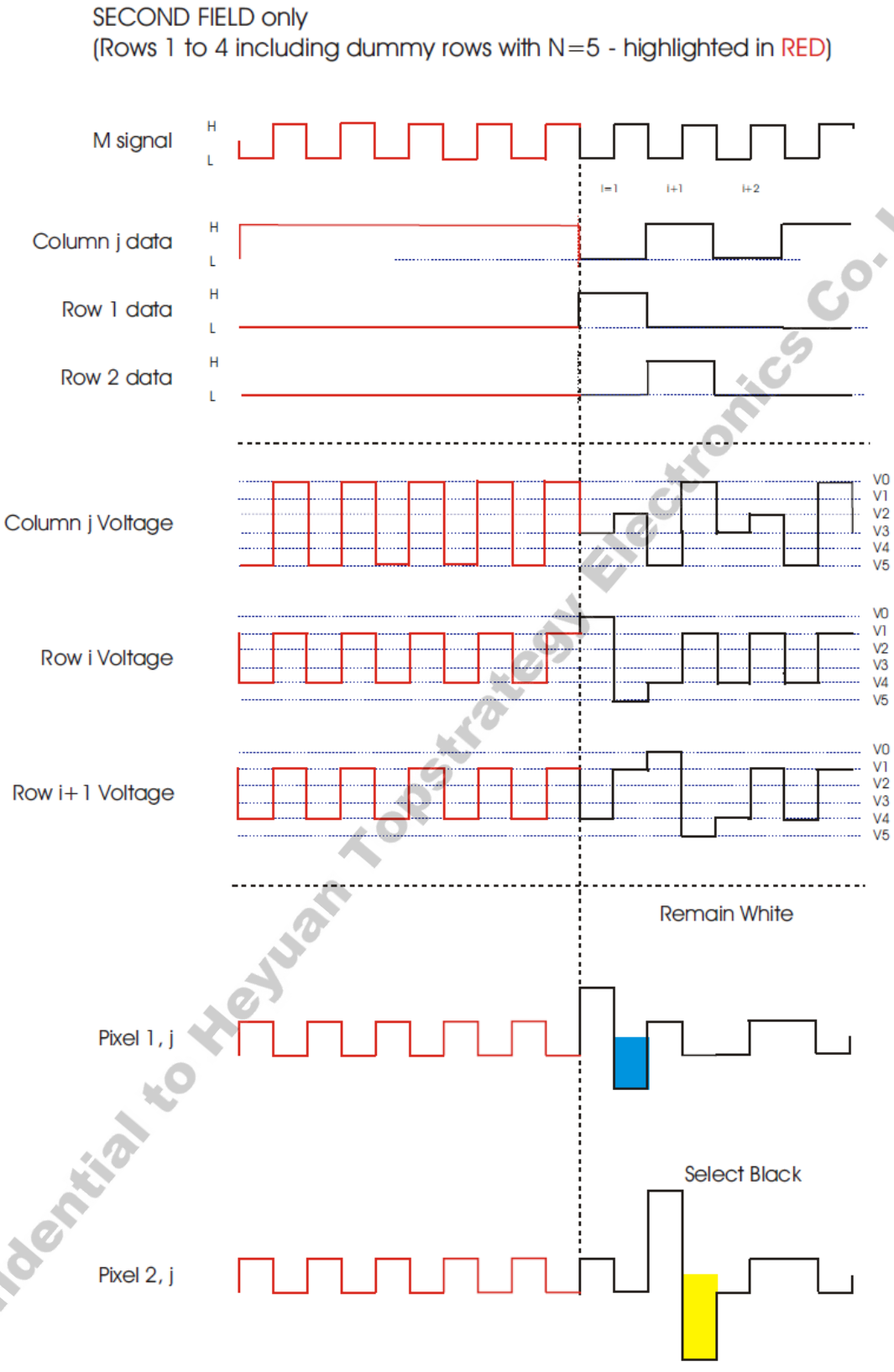


Figure 8-3: Illustration of how dummy rows preceding row 1 are generated.

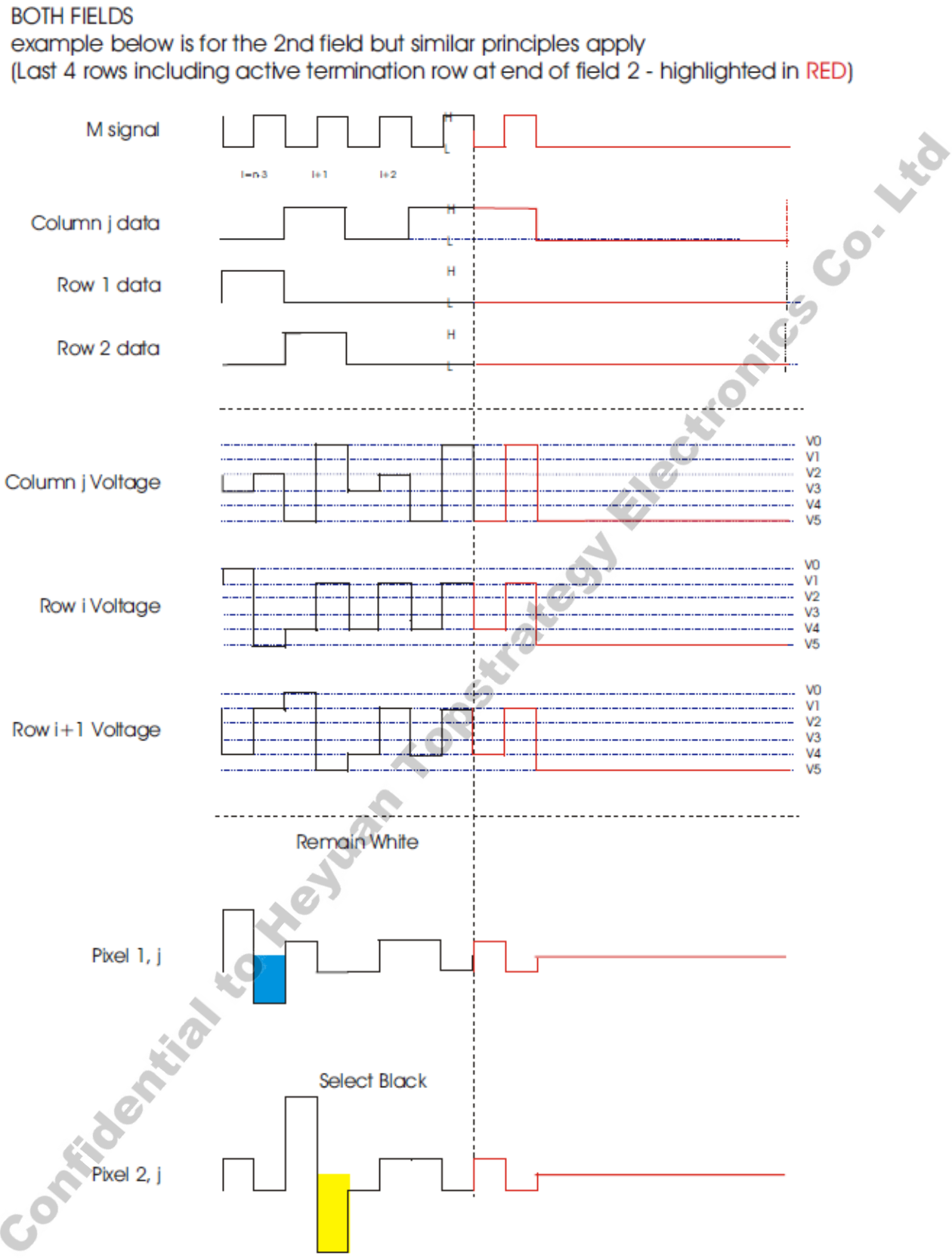
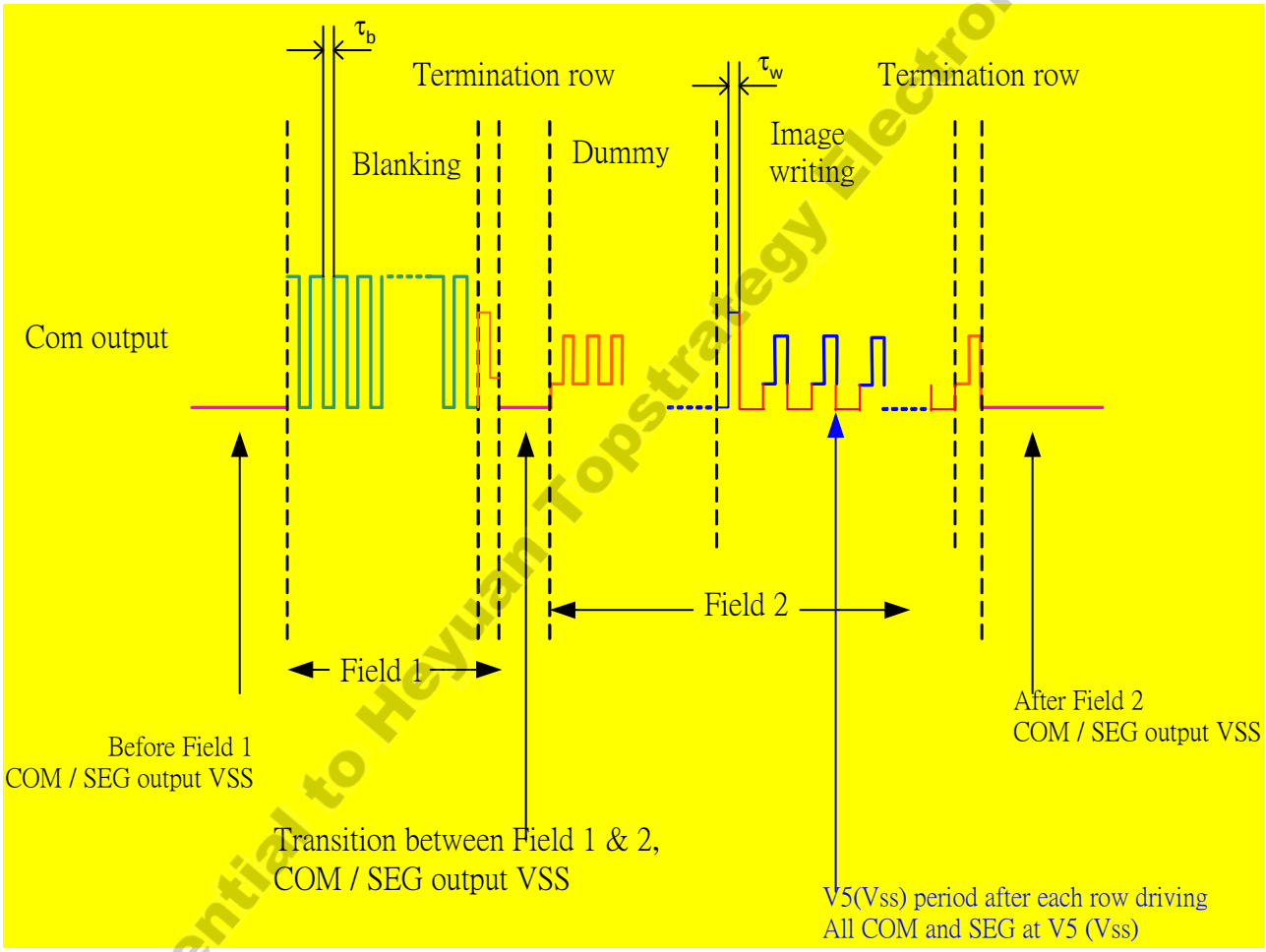


Figure 8-4: Illustration of how dummy rows are generated at last 4 rows.

Remark:

- Both dummy and termination rows, when active, should output voltages consistent with applying the following data to the COM and SEG:
- COM data = 0
- SEG data = 1
- The relevant voltages should correspond to the specific field that the dummy or termination rows occur in, e.g. the termination row at the end of the 1st field should apply the COM and SEG voltages relevant to the 1st field.

Figure 8-5: A complete update sequence



8.1 Data mapping truth table

Figure 8-6 : Segment mapping

SEG mapping

Data	M	First field data	Output Field 1	Field 2
1	1	0 (Disable)	V0	V0
1	0	0	V5	V5
0	1	0	V0	V2
0	0	0	V5	V3
1	1	1 (Enable)	V0	V0
1	0	1	V5	V5
0	1	1	V2	V2
0	0	1	V3	V3
Dummy & termination rows				
1	1	0 (Disable)	V0	V0
1	0	0	V5	V5
1	1	1 (Enable)	V0	V0
1	0	1	V5	V5

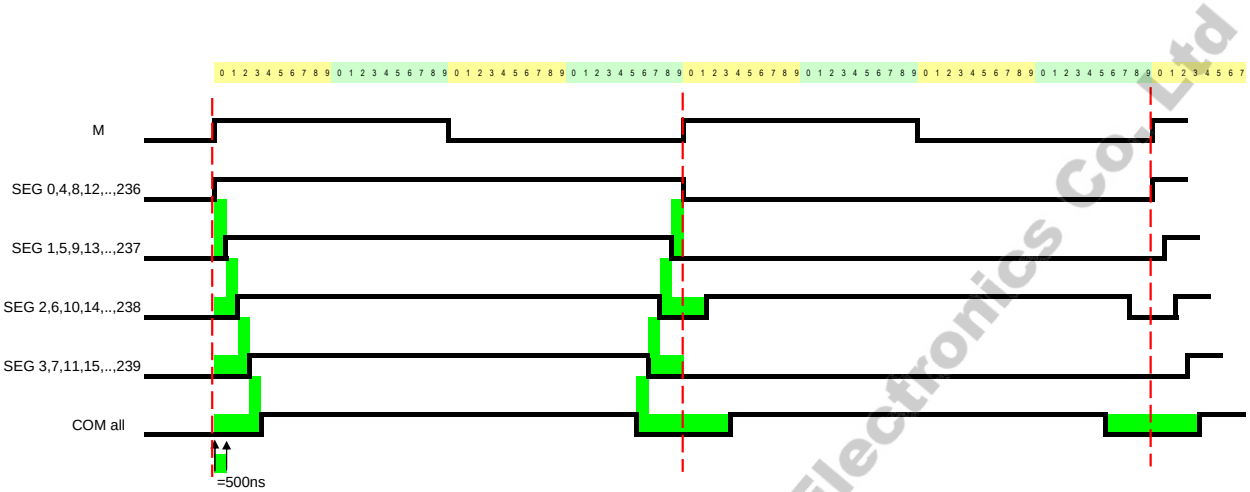
Figure 8-7 : Common mapping

COM mapping

Data	M	First field data	Field 1	Field 2
1	1	0 (Disable)	V5	V5
1	0	0	V0	V0
0	1	0	V0	V1
0	0	0	V5	V4
1	1	1 (Enable)	V5	V5
1	0	1	V0	V0
0	1	1	V1	V1
0	0	1	V4	V4
Dummy & termination rows				
0	1	0 (Disable)	V0	V1
0	0	0	V5	V4
0	1	1 (Enable)	V1	V1
0	0	1	V4	V4

8.2 Non-overlapping period

Figure 8-8 : Illustration of Segment non-overlapping



Non overlapping features between SEG / COM are added for power saving. This feature can be disable by command.

9 Command Table

Table 9-1: Register Summary

Reg	Description	R/W	Byte sequence	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x00	UPDATE	W	One byte command								
0x01	NUMROWS	R/W	0	NUMROWS[7:0]							
0x02	NUMCOLS	R/W	0	NUMCOLS[7:0]							
0x03	IMGORIENT	R/W	0							COL DIR	ROW DIR
0x04	IMGIDX	R/W	0	COL ADDRESS[7:0]							
			1	ROW ADDRESS[7:0]							
0x05	IMGMEM	R/W	0-2879	Databyte							
0x06	OTPWRITE	W	0						OTPWRITE[2:0]		
0x07	LUTVERS	R	0	LUTVERS[7:0]							
			1	LUTVERS[15:8]							
0x08	TEMPREG	R/W	0	TEMPREG[7:0]							
0x09	DISP_OPTION	R/W	0							B_SEN EN	DSLP EN
0x0A	VERSION	R	0	VERSION[7:0]							
			1	VERSION[15:8]							
0x0B	STATUS	R	0	DISP BUSY	OTP BUSY						
0x0C	LUTOVERRIDE	R/W	0	Tw[7:0]							
			1	Vs+Vd[6:0]							Tw[8]
			2	Tb[7:0]							
			3	Vd[1:0]		Vb[4:0]					Tb[8]
			4					Reserved	Vd[4:2]		
0x0D	PREDEFTYP	R/W	0				CHK[2:0]			IMGTYP[1:0]	
0x0E	PARTUPDATE	R/W	0		Start Row[6:0]						
			1		NumberRow[6:0]						
0x10	UPDATECNT	R	0	UPDATECNT[7:0]							
			1	UPDATECNT[15:8]							
			2	UPDATECNT[23:16]							
			3	UPDATECNT[31:24]							
0x11	DUMMYROWS	R/W	0	TERM Row	F1 Data EN	ExtraLine EN	DummyRow[4:0]				
0x12	ABORT	W	One byte command								
0x13	Reserve	W	-								
0x14	DEEP SLEEP	W	One byte command								
0x16	MCONF	R/W	0								MCONF
0x17	TEMPCAL	R/W				TEMPCAL[5:0]					
0x18	TEST COMMAND	R/W	0	R_LATCH EN	0	0	0	0	0	0	0
			1	0	0	0	0	0	0	0	0
			2	0	0	0	0	0	0	0	0
			3	1	1	0	0	0	0	0	0
			4	0	1	0	0	0	1	0	1
			5	1	0	0	0	0	1	1	0
			6	0	1	0	0	0	0	0	0
0x19	Reserve	W	-								
0x1A	OTP Dump	W	One byte command								
0x1B	Reserve	R/W	-								
0x1C	Reserve	R/W	-								
0x1D	ANASETTING	R/W	0	Analog block control byte							
			1	Analog block control byte							
			2	Analog block control byte							
			3	Analog block control byte							
			4	Analog block control byte							
			5	Analog block control byte							
			6	Analog block control byte							
0x1E	Reserve	W	-								
0x1F	Reserve	W	-								

Table 9-2: Command Description

Offset	Register	R/W	Description	Details
0x00	UPDATE	W	Update Display	A write of any value to this single-byte command causes the ASIC to perform a full, partial or predefined display update. On completion of an update the ACK pin will be pulsed low. During display update, STATUS can be used to determine when the update will be completed. The normal procedure would be to download an image to internal memory using the IMGIDX & IMGMEM registers, set any optional parameters e.g. PARTUPDATE, TEMPREG, LUTVALUES, PREDEFIMG etc. before issuing an Update Display command. TEMPREG must be written before UPDATE command. This command performs a full display update using it's temperature register value to get the Vblank, Vstrobe, Vdata, Tblank & Twrite values from the internal LUT. After an UPDATE (0x00) command, it should wait for 500 micro-seconds to read the DISP BUSY (bit 7 in 0x0B), display update will complete after DISP BUSY turns from 1 to 0. Or by monitoring the ACK pin signal to know the display update status. Figure 9-1 illustrates the flow of UPDATE
0x01	NUMROWS	R/W	Number of rows	A write to this register overrides the value held in the NUMROWS OTP variable for the next UPDATE command. The register will be reset to the value held in the OTP NUMROWS variable after the UPDATE command is completed. A read from register will return the value held in the NUMROWS OTP variable. It is read by the microcontroller to determine the display size and automatically configure software based on the size of display attached. Byte 0, Bits[7:0] = Number between 8 and 96
0x02	NUMCOLS	R/W	Number of columns	A write to this register overrides the value held in the NUMCOLS OTP variable for the next UPDATE command. The register will be reset to the value held in the OTP NUMCOLS variable after the UPDATE command is completed. A read from register will return the value held in the NUMCOLS OTP variable. It is read by the microcontroller to determine the display size and automatically configure software based on the size of display attached. Byte 0, Bits[7:0] = Number between 1 and 240 **Remark:** NUMCOLS setting only control the data writing to restricted RAM address. All SEG, including those beyond NUMCOLS limit, do have output waveform regardless of NUMCOLS setting.
0x03	IMGORIENT	R/W	Orientation of image	Allows the Host Controller to configure the orientation of the image to be displayed on the display. By default, image stored in the Internal Image Memory will be displayed with the initial row and column (0/0) being in the top left corner of the

Offset	Register	R/W	Description	Details
				display. A write to this register overrides the value held the in IMGORIENT OTP variable until the driver IC is placed in DEEPSLEEP or RESET. An UPDATE command will not reset the value. Bit 0 sets the row direction: A value of 0 causes the Internal Image Memory to be updated from row 0 to row NUMROWS - 1. A value of 1 causes the Internal Image Memory to be updated from row NUMROWS - 1 to row 0 Bit 1 sets the column direction: A value of 0 causes the Internal Image Memory to be updated from column 0 to column NUMCOLS - 1. A value of 1 causes the Internal Image Memory to be updated from column NUMCOLS - 1 to column 0. As each data byte contain 8 pixel image data. The NUMCOLS address is shift in a step of 8 every time. Bits 2-7 are undefined and should be set to 0. Note: This command should be issued before IMGMEM memory writes to have the display image flipped correctly as desired.
0x04	IMGIDX	R/W	Image Index	This command consecutively writes two byte of data (Column Address, Row Address) into registers as an index into the Image Memory. Byte 0, Bits [7:0] = Column address: 0 to NUMCOLS - 1 Byte 1, Bits [7:0] = Row address: 0 to NUMROWS - 1 Before initiating a write or read to/from Image Memory the IMGIDX register should be set to the offset into the image that is to be transferred to/from Image Memory. This has the effect of resetting the Internal Image Memory pointer to the desired offset. The IMGIDX register need only be written once for each image transfer. The driver IC will provide an optimized Image Memory write operation whereby this register only has to be written once to set the index, from then on every write/read to/from the IMGMEM register will provide the next byte in memory. This allows for situations where the microcontroller is getting the Image packet at a time of the communications network and is able to stream each data packet into the driver IC without having to set up the index between each communications packet received. In normal operation the microcontroller would set this register to (0,0) at the start of an image download and then write a constant stream of bytes to IMGMEM as each packet of data arrives over the communications network. The driver IC would be placed into SLEEP mode between each data packet that arrives over the network. After an UPDATE command, (0,0) is necessary to send in IMGIDX to clear the IMGIDX register for next display update. The memory is written and read in byte format. During memory read / write, even if the column address is not a multiple of 8. i.e. the last 3 bits is not 000. The last 3 bits of column address will still be treated as 0 so data is written / read in the whole memory byte. If IMGORIENT, NUMROWS, NUMCOLS had been altered, the value in IMGIDX will no longer be valid.
0x05	IMGMEM	R/W	Image Memory	Each write to this register places a byte of data into the Image Memory and set the internal Image Memory pointer address to next byte according to the setting in IMGORIENT Each read from this register reads a byte of data from the Image Memory at the internal Image Memory pointer location and set the internal Image

Offset	Register	R/W	Description	Details
				Memory pointer to next byte according to the setting in IMGORIENT The first byte output from reading the IMGMEM register will be a dummy byte. The internal Image Memory pointer can be set or reset at any time using the IMGIDX register. The address pointer is always increasing. If Column address has reached its boundary defined as NUMCOLS-8, the Column address will be wrapped around to 0 and row address will be offset by 1 accordingly. The increment or decrement of row address will depend by IMGORIENT setting. If Row address counter reached its boundary as defined as NUMROWS-1, it will be wrapped around to 0. The microcontroller can optimize the reading or writing of image data to the image memory by reading or writing multiple data bytes to this register whilst keeping the Chip Select (CS) pin enabled. Each subsequent data byte that is read/written will be read/written from/into the next image memory location as defined by the Internal Memory Pointer. The microcontroller can continue to read/write data until either the end of image memory is reached or the Chip Select pin is disabled. In normal operation this memory is used to store full or partial images that shall be written to the display, but during unit test this memory can be used to store the contents of the OTP memory before being written using OTPWRITE command. **NOTE 1**: During a Display Update the Image Memory cannot be accessed. **NOTE 2**: Memory access should only be performed after proper setting of NUMROWS, NUMCOLS, and IMGORIENT. **NOTE 3:** When using the Image Memory for writing to the OTP the values of NUMROWS and NUMCOLS must first be set to 96 and 240 respectively.
0x06	OTPWRITE	W	Copy the contents of the Image Memory to OTP memory	A write to this register causes the contents of the Image Memory to be written to the OTP memory. One byte (byte A) parameter is required for this command. Default of Byte A is 0x00, which enable OTP write for customer OTP sector. (OTPADDR[0-468]) Write 0x01 in Byte A will enable OTP write for production reserved sector. (OTPADDR[469-489]) Write 0x02 or 0x03 in Byte A will enable OTP write for entire OTP sector. (OTPADDR[0-511]). When using this option, user should write 1s to all bits in the address of OTPADDR[469-489] to prevent corruption of production data. This command can only be performed once. The OTP memory can only be written as a complete memory image. No partial, or specific byte writes are possible. A separate supply voltage will be required to update the OTP. This will not be generated internally and must be supplied externally. **NOTE:** The OTP memory is non-volatile write once memory. It is expected to be written during LCM Test and never changed. After an OTPWRITE (0x06) command, it should wait for 500 micro-seconds to read the OTP BUSY (bit 6 in 0x0B). Data will be complete written in to OTP after OTP BUSY turns from 1 to 0 or by monitoring the ACK pin signal.

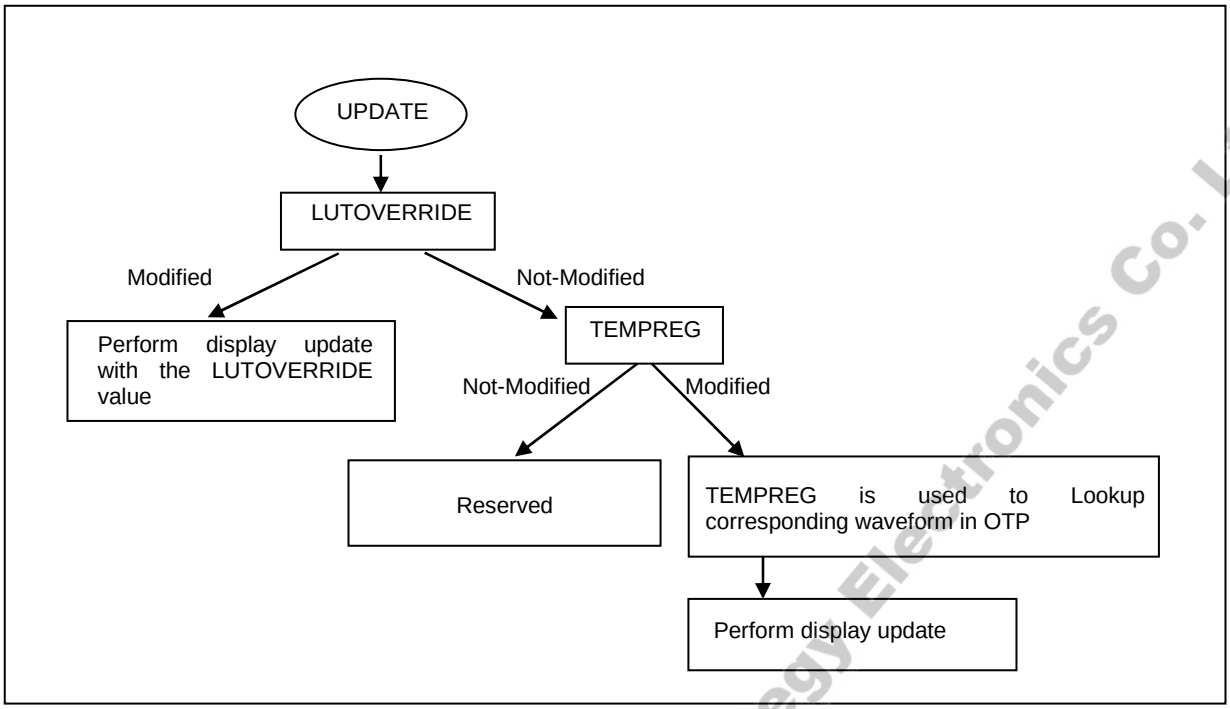
Offset	Register	R/W	Description	Details
0x07	LUTVERS	R	LUT Version	A read from this 16 bit register will return the LUT header information indicating the version of the installed LUT.
0x08	TEMPREG	R/W	Temperature	A read from this register will return the content which stored in TEMPREG and the value in this register will not be changed. A write to this register will override the existing temperature value. The value will be used as the index to the Indirect LUT on the next display update command. There has an internal flag to indicate that the overridden TEMPREG value should be used in the next display update and this flag will be cleared after display update command. Also, the value stored in register will be cleared at the completion of • ABORT command; or • Reset from DEEPSLEEP. This value will not be reset during wakeup from SLEEP mode. The flow of UPDATE is shown in the Figure 9-1
0x09	DISPOPT	R/W	Display options configuration	The command control the optional sequence for display UPDATE command Bit [0] = 0: Return to IDLE mode after completion of UPDATE command (Default) Bit [0] = 1: Enter DEEPSLEEP mode after completion of UPDATE command Bit [1]: Reserved Bit [4]: Reserved The setting of this command will not be reset by display UPDATE, ABORT or WAKEUP. It will be reset to default by HW reset.
0x0A	VERSION	R	Driver IC Version	A read from this 16-bit register will return the current version of the driver IC. Bit [7:0]: Minor version Bit [15:8]: Major version The value is set as 0x0200
0x0B	STATUS	R	Driver IC Status	A read from this register will return the current status of the driver IC. Bit [7] - Display busy (active HIGH) Bit [6] - OTP busy (active HIGH) Bit [5] – Reserved For BUSYFLAG related command such as Display busy, OTP busy, below is the busy flag sequences: 1) Send BUSY related command 2) Read corresponding BUSY flag after 500us 3) If BUSY flag still = 1, continuous to wait and read BUSY flag. 4) Do next step after read back the status flag = 0
0x0C	LUTOVERRIDE	R/W	Override LUT Values	A write to this register will set the Vblank, Vstrobe, Vdata, Tblank & Twrite values to be used on the next display update. These values are

Offset	Register	R/W	Description	Details
				used in preference to the internal LUT values. There is an internal flag to indicate that the overridden LUTOVERRIDE value should be used in the next display update and the flag will be cleared after display update command or HW reset. The stored value in this register will be cleared after HW reset. Only if the transfer of the LUT (5 bytes) is completed, the register will be updated. If the data transfer is interrupted before completion, the data will be discard and the register will not be updated See **Table 7-6** for details of the format for the data to be supplied for this command. Note: As the ASIC will search for one set of appropriate LUT during update, the current value stored in LUTOVERRIDE may not reflect what parameters will be used in the next update.
0x0D	PREDEFTYP	R/W	Predefined Image type	A write to this register will set the type of predefined image that will be written to the display on the next Predefined Image Update command. There is an internal flag to indicate that the overridden PREDEFTYP value should be used in the next display update and the flag will be cleared after display update command, HW reset or reset from DEEPSLEEP. The stored value in this register will be cleared after HW reset or reset from DEEPSLEEP. This register will not affect the IMGMEM content. The value will be cleared at the completion of the next UPDATE command. A write to this register will overwrite the image held in IMGMEM with the selected predefined image. Bits [1:0]: Image type: [00] = Black [01] = White [10] = Chequerboard [11] = Undefined Bits [4:2]: Chequerboard size: [000] = 1x1 pixel [001] = 2x2 pixel [010] = 4x4 pixel [011] = 8x8 pixel [100] = 16x16 pixel [101] = 32x32 pixel [110] = 64x64 pixel [111] = Undefined Bits [5:7] Undefined
0x0E	PARTUPDATE (16 bit)	R/W	Partial image update parameters	A write to this register will set the Start Row for the Display Update command. The value will be cleared at the completion of the next UPDATE command, HW reset, or reset from DEEPSLEEP mode. The value is not affected by wakeup from SLEEP mode First byte Bits [0-6]: Start row, available range is 0 to 95. Bits [7]: NA Second byte

Offset	Register	R/W	Description	Details
				Bits [8-14]: Number of rows, available range is 1 to 96. Bits [15]: NA During a Partial Update, the row data will keep at low logic level for the inactive rows i.e. the rows before the start row and after the end row. For partial update, the dummy rows ahead of the second field, and the extra row at the end of the second field, will be applied immediately prior to the Start row (not necessarily row 0) and after the last addressed row (Start row + Number of rows - 1, not necessarily row n), respectively.
0x10	UPDATECNT (32 bits)	R	Display update count	A read from this register will return the total number of display updates performed since the last power down. This register shall not be reset to 0 when by a HW reset or when going into DEEPSLEEP.
0x11	DUMMYROWS (8 bits)	R/W	Dummy row count	A write to this register overrides the value held in the First field data, Dummy rows and termination row at end of fields 1&2 OTP variables for the next UPDATE command. The register will be reset to the value held in the OTP variables after the UPDATE command is complete. A read from register will return the value held in the First field data, Dummy rows and termination row at end of Fields 1 & 2 OTP variables. Bits [0-4]: Dummy row count (0 to 31) Bits [5]: Enable/Disable Extra line address time 0: Disable Extra line address time 1: Enable Extra line address time Extra line address time is a 2x τ_w period after each image writing line, which all COM and SEG will be pulled to VSS level. Bit [6] Enable/Disable first field data 0: Disable first field data. Vd = 0v 1: Enable first field data. Vd = Vd Bit [7] Termination row at end of Fields 1 & 2 1: Enable, 1 termination row will be completed at the end of each field 0: Disable, No termination row will be issued If the Dummy Row count is set then the dummy rows are only added to the start of field 2. Field 1 remains unchanged. If the termination row at the end of fields 1 & 2 is set then an extra row is output at the end of both field 1 and field 2. During the dummy and termination rows, COM data=0, SEG data=1.
0x12	ABORT (8 bits)	W	Abort	A write to this register will abort any current action in progress in the driver IC except OTPWRITE. If an ABORT command is received by the driver IC during an UPDATE then only the current row is completed to ensure the display is left in a DC Balanced state. Termination rows will not be added. The sequence of actions by the driver IC is as follows: finish current row, update registers, turn off power, send ACK pulse. All registers will be left in the same state as if the update had completed successfully. IMGMEM contents are retained. All voltage generation logic will be reset. Register 0x03, 0x09, 0x10 are not being reset Note: The content of OTP cannot be guaranteed when performing "ABORT" during OTP update.

Offset	Register	R/W	Description	Details
0x13	Reserved	-	Reserved	Reserved
0x14	DEEPSLEEP	W	Enter deep sleep mode	This is a one byte command instructing the driver IC to enter a low power Deep Sleep mode. In this mode the driver IC will consume the minimum amount of power possible. RES# pin should keep high. For the device to exit from DEEPSLEEP mode, a hardware RESET must be performed. After reset, all temporary registers will be reset to defaults held in OTP memory and the driver IC will return to an idle state waiting to receive further commands.
0x15	Reserved	-	Reserved	Reserved
0x16	MCONF	R/W	M Configuration	This register allows the Host Controller to set the starting polarity of signal M/FR. The options are: Bit 0 = 0: Start M/FR signal Low Bit 0 = 1: Start M/FR signal High The register will be reset to the value held in the OTP M/FR variable after the UPDATE command is complete.
0x17	TEMPCAL	R/W	Reserved	Reserved
0x18	Test command: TESTCMD	R/W	Test command	This is a test command. **Default parameter** 00, 00, 00, C0, 45, 86, 40 **Segment non-overlapping disable** 80, 00, 00, C0, 45, 86, 40
0x19	Reserve	W		
0x1A	OTP Dump	W	OTP contents dump	This command loads the content of the OTP into display RAM. IMGIDX (Reg04) need to be set as (0,0) for RAM address counter initialization before running this command After an OTP Dump (0x1A) command, it should wait for 500 micro-seconds to read the OTP BUSY (bit 6 in 0x0B), data will be ready to read after OTP BUSY turns from 1 to 0. Or by monitoring the ACK pin signal, read the OTP content in GDDRAM when low pulse is detected.
0x1B	Reserve	R/W		
0x1C	Reserve	R/W		
0x1D	Test command: ANASETTING	R/W	Analog blocks control	This command follows by parameters **Default parameters:** A5, 80, 00, F1, 4C, 07, 08 Setting written to this register will be returned to default after SLEEP, DEEPSLEEP and Reset. The overiding setting will be kept after UPDATE The default value is OTP programmable by IC vendor. The corresponding address is otpaddr[478:484]
0x1E	Reserve	W		
0x1F	Reserve	W		

Figure 9-1: Update Flow



10 OPERATION SEQUENCES

10.1 Display update

Table 10-1: Operation sequence of initial power-up

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI supply)	
	IC	-	POR	

Table 10-2: Operation sequence of a display update

Sequence	Action by	Command	Action Description	Remark
1	User	-	HW reset	
	IC	-	Turn on VDD regulator	
	IC	-	OTPBUSY High	
	IC	-	Oscillator ON	
	IC	-	Load register with OTP value	
	IC	-	OTPBUSY Low	
	IC	-	ACK H	
	IC	-	Oscillator OFF	Enter IDLE mode
2	User	0x01	NUMROWS	Optional
	User	0x02	NUMCOLS	Optional
	User	0x03	IMGORIENT	Optional
	User	0x04	IMGIDX	Optional
	User	0x05	IMGMEM	
	User	0x07	LUTVERS	Optional
	User	0x08	TEMPREG	Optional
	User	0x09	DISPOPT	Optional
	User	0x0A	VERSION	Optional
	User	0x0B	STATUS	Optional
	User	0x0C	LUTOVERRIDE	Optional
	User	0x0D	PREDEFTYP	Optional
	User	0x0E	PARTUPDATE	Optional
	User	0x10	UPDATECNT	Optional
	User	0x11	DUMMYROWS	Optional
	User	0x16	MCONF	Optional
3	User	0x00	UPDATE	Enter Update Mode
	IC	-	DISPLAYBUSY High	After issued 0x00, it should wait 500us to read the DISPLAYBUSY.
	IC	-	Oscillator On	
	IC	-	UPDATECNT + 1	
	IC	-	VREG On	
	IC	-	Load corresponding waveform LUT	Optional
	IC	-	Booster and Bias On	
	IC	-	First Field display	
	IC	-	Termination Row	
	IC	-	Dummy Row	
	IC	-	Second Field Display	
	IC	-	Termination Row	
	IC	-	Finish Update	
	IC	-	Booster and Bias Off	
	IC	-	VREG Off	
	IC	-	Reset register value	
	IC	-	DISPLAYBUSY Low	

	IC	-	ACK Negative Pulse	**ACK L if Enter DEEP SLEEP mode.**
	IC	-	Oscillator Off	Enter IDLE Mode
	IC	-	Enter DEEP SLEEP mode	Optional

10.2 OTP programming

Table 10-3: Operation sequence of OTP programming

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power VCI and VPP	
	IC	-	Reset and enter IDLE mode	
2	User	0x01	Set ram window, x=96	
	User	0x02	Set ram window, y=240	
	User	0x03	set IMGORIENT = 0x00	
	User	0x04	Initial ram address pointer as (0,0)	
	User	0x05	IMGMEM, Memory Writing.	
	User	0x04	Initial ram address pointer as (0,0)	
3	User	0x06	OTPWRITE	After issued 0x06 command, it should wait 500us to read the OTPBUSY.
	IC	-	OTPBUSY H	
	IC	-	Oscillator On	
	IC	-	Program OTP	
	IC	-	OTPBUSY L	
	IC	-	ACK Negative Pulse	
	IC	-	Oscillator Off	
	IC	-	IC Enter IDLE mode	

10.3 OTP dumping

Table 10-4: Operation sequence of dumping OTP content into RAM

Sequence	Action by	Command	Action Description	Remark
			IC at IDLE mode	
1	User	0x01	set ram window, x=96	
	User	0x02	set ram window, y=240	
	User	0x03	set IMGORIENT = 0x00	
	User	0x04	Initial ram address pointer as (0,0)	
2	User	0x1A	OTPDUMP	After issued 0x1A command, it should wait 500us to read the OTPBUSY.
	IC	-	Oscillator On	
	IC	-	Dump OTP data to RAM	
	IC	-	ACK Negative Pulse	
	IC	-	Oscillator Off	
3	User	0x04	Initial ram address pointer as (0,0)	
4	User	0x05	IMGMEM, Memory Reading	
			IC Enter IDLE mode	

10.4 Entering SLEEP mode

Table 10-5: Operation sequence of entering SLEEP mode

Sequence	Action by	Command	Action Description	Remark
			IC at IDLE mode or Operating mode	
1	User	-	Pull Low IDLE/SLEEP pin.	
	IC	-	Wait until the current operation, if any, is completed	
	IC	-	ACK L	
	IC	-	VDD regulator Off	
			IC enter SLEEP mode	

10.5 Entering DEEP SLEEP mode

Table 10-6: Operation sequence of entering DEEP SLEEP mode

Sequence	Action by	Command	Action Description	Remark
			IC at IDLE mode or Operating mode	
1	User	0x14	DEEP SLEEP enable command	
	IC	-	Wait until the current operation, if any, is completed	
	IC	-	ACK L	
	IC	-	VDD regulator Off	
			IC enter DEEP SLEEP mode	

11 ABSOLUTE MAXIMUM RATINGS

Table 11-1: Maximum Ratings

(Voltage Reference to V_{SS} = 0V)

Symbol	Parameter	Value	Unit
V_{CI}	Supply Voltage	-0.3 to +4.0	V
V_H	Supply Voltage	-0.3 to 42	V
V_{in}	Input Voltage	V_{SS} -0.3 to V_{DDIO} +0.3	V
T_A	Operating Temperature	-30 to +80	ºC
T_{STG}	Storage Temperature Range	-65 to +150	ºC

Maximum Ratings are those beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

11.1 ESD Tolerance

JEDEC22A

- Machine Model 100V
- Human Body Model 2000V

12 DC CHARACTERISTICS

Conditions:

Voltage referenced to $V_{SS,}$ V_{CI} = 3.0V, T_A = 25°C

Table 12-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min	Typ	Max	Unit
V_{DD}	Core logic Power supply	-	V_{DD}	1.65	1.8	1.95	V
V_{DDIO}	MCU interface level	-	V_{DDIO}	VDD		VCI	V
V_{CI}	Power supply	-	V_{CI}	2.0	-	3.8	V
V_0	Panel driving power range	-	V_0	8.25	-	40	V
V1	Panel driving voltage range	-	V1	10	-	40	V
V2	Panel driving voltage range	-	V2	5	-	40	V
V3	Panel driving voltage range	-	V3	0	-	20	V
V4	Panel driving voltage range	-	V4	0	-	10	V
Vpp	OTP programming voltage supply	-	Vpp	7.25	7.5	7.75	V
Ivpp	OTP programming current supply	-	Vpp	-	-	15	mA
V_{OH}	Logic High Output Voltage	IVOUT = -100uA	MCU interface pins	0.9* V_{DDIO}	-	V_{DDIO}	V
V_{OL}	Logic Low Output Voltage	IVOUT = 100uA	MCU interface pins	0	-	0.1* V_{DDIO}	V
V_{IH}	Logic High Input voltage		MCU interface pins	0.8* V_{DDIO}	-	V_{DDIO}	V
V_{IL}	Logic Low Input voltage		MCU interface pins	0	-	0.2* V_{DDIO}	V
I_{DSLP}	Deep Sleep mode Current	V_{CI}=3.0V, Osc OFF , VDD regulator off, Booster off, No panel attached	VCI	0	1	2	uA
I_{SLP}	Sleep mode Current	V_{CI}=3.0V, Osc OFF , VDD regulator off, Booster off, No panel attached SLEEP = L	VCI	0	1	2	uA
I_{DP1}	Display Mode Supply Current	V_{CI} = 3.0V, V0 = 30V, Charge Pump On, Bias Voltage Buffer Off, No driving Update	V_{CI}	-	1	1.5	mA
Ron	SEG / COM On resistance	V0 = 30V, Vout = 15V	COM0 ~ COM95 SEG0 ~ SEG239		5		kohm
Vout	Booster output voltage			20		42	V
Iout	Booster loading	V0 set to 30V or below, dV < 0.5V				1.0	mA
Iout	Booster loading	V0 set to 30V to 40V, dV < 0.5V				1.0	mA

13 AC CHARACTERISTICS

13.1 Oscillator

Table 13-1: Oscillator characteristics

Conditions: No panel loading

Symbol	Parameter	Test Condition	Min.	Typ.	Max	Units
Fosc	Oscillator frequency	VCI = 3.0V, 25°C	0.95	1	1.05	MHz
Fosc	Oscillator frequency	VCI = 2.0 to 3.8V, Temperature = -30 to +80°C	0.85xF	F	1.15xF	

13.2 Booster start up

Table 13-2: Booster characteristics

Conditions: No panel loading

Symbol	Parameter	Test Condition	Min.	Typ.	Max	Units
$I_{VCIpeak}$	Booster peak current	V0 = 30V VCI = 2.2V 1mA loading at V0			40	mA
I_{VCI}	Booster average current	V0 = 30V VCI = 2.2V 1mA loading at V0		35		mA
$I_{VCIpeak}$	Booster peak current	V0 = 40V VCI = 2.5V 1mA loading at V0			45	mA
I_{VCI}	Booster average current	V0 = 40V VCI = 2.5V 1mA loading at V0		40		mA
$I_{VCIpeak}$	Booster peak current	V0 = 40V VCI = 2.5V 1.5mA loading at V0			65	mA
I_{VCI}	Booster average current	V0 = 40V 1.5mA loading at V0		60		mA
Indpeak	Inductor peak current				200	mA

13.3 Interface timing

Table 13-3: DEEPSLEEP/SLEEP/IDLE Timing Characteristics

Parameter	Min	Typ	Max	Unit
IDLE to SLEEP		1		µs
SLEEP to IDLE		1000		µs
DEEPSLEEP Command to DEEPSLEEP		1		µs
DEEPSLEEP to IDLE		1000		µs

Table 13-4: SPI Timing Characteristics (VDD=1.8V, Temperature = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency			10	MHz
tsp	CS# low to positive edge on SCLK, in active mode	20			ns
tch	SCLK Clock high	50			ns
tcl	SCLK Clock low	50			ns
tr	SCLK clock rise time			5	ns
tf	SCLK clock fall time			5	ns
tsu	Setup data before positive edge on SCLK	20			ns
thd	Hold data after positive edge on SCLK	20			ns
tcq	Negative edge on SCLK to SO output			30	ns
tns	Negative edge on SCLK to CS# high	20			ns
tsz	Positive edge on CS# to SO Hiz			20	ns
tss	CS# deselect time	100			ns

Figure 13-1: SPI Timing Diagram (Write operations)

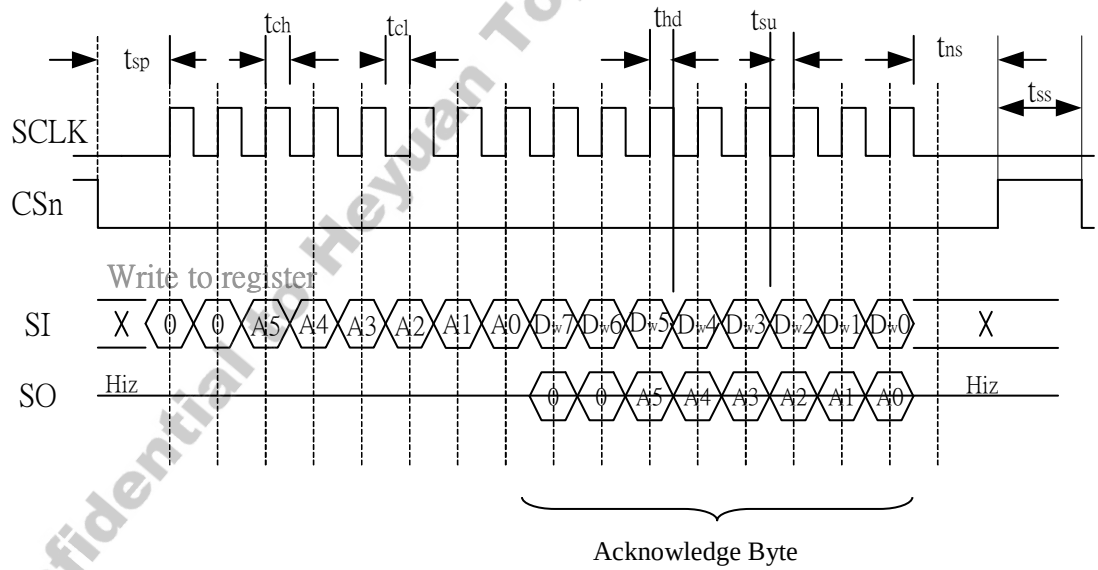


Figure 13-2: SPI Timing Diagram (Read operations)

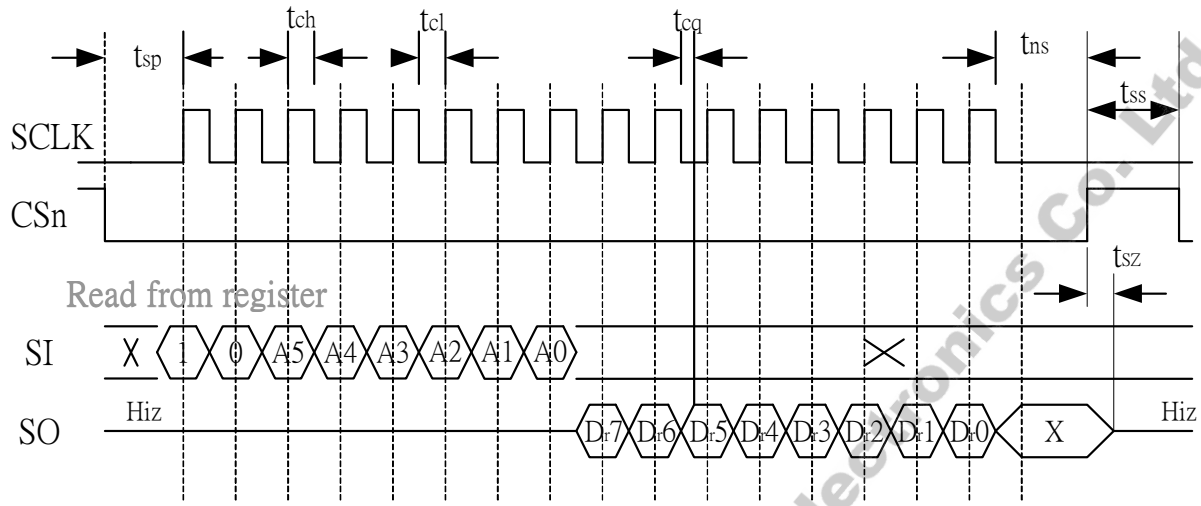
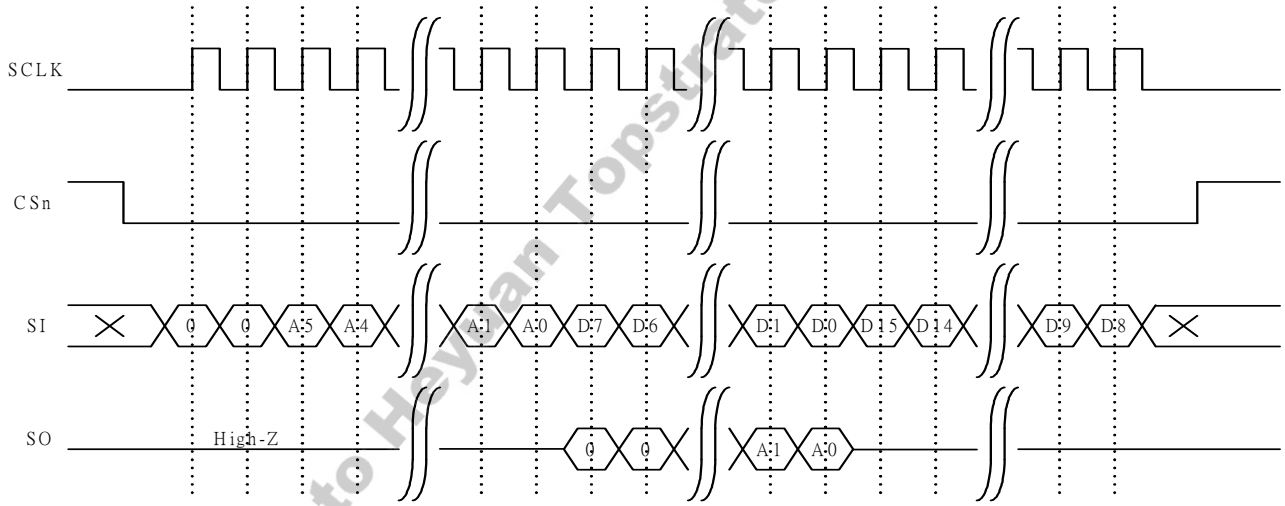


Figure 13-3: SPI Timing Diagram (16-bit Write Operation)



Note: Address Byte is echoed back on SO during Write of first Byte .

Figure 13-4: SPI Timing Diagram (16-bit Read Operation)

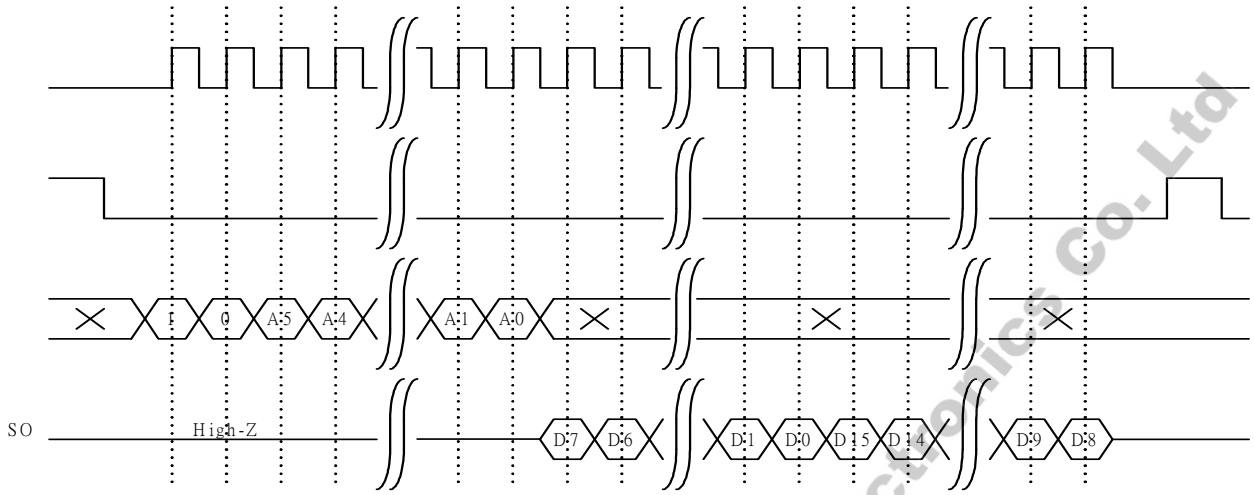
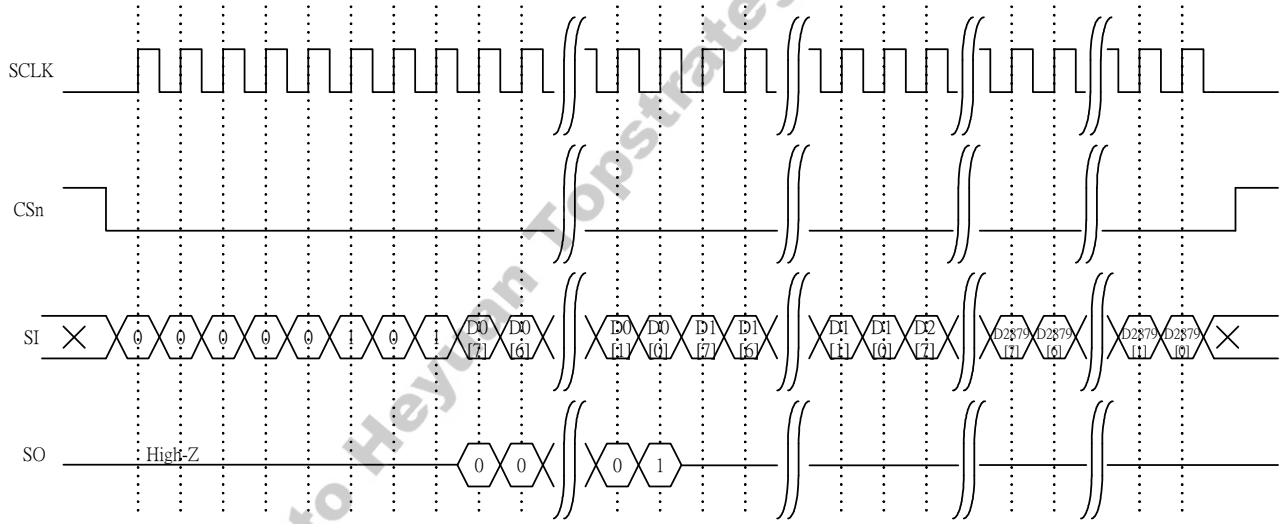
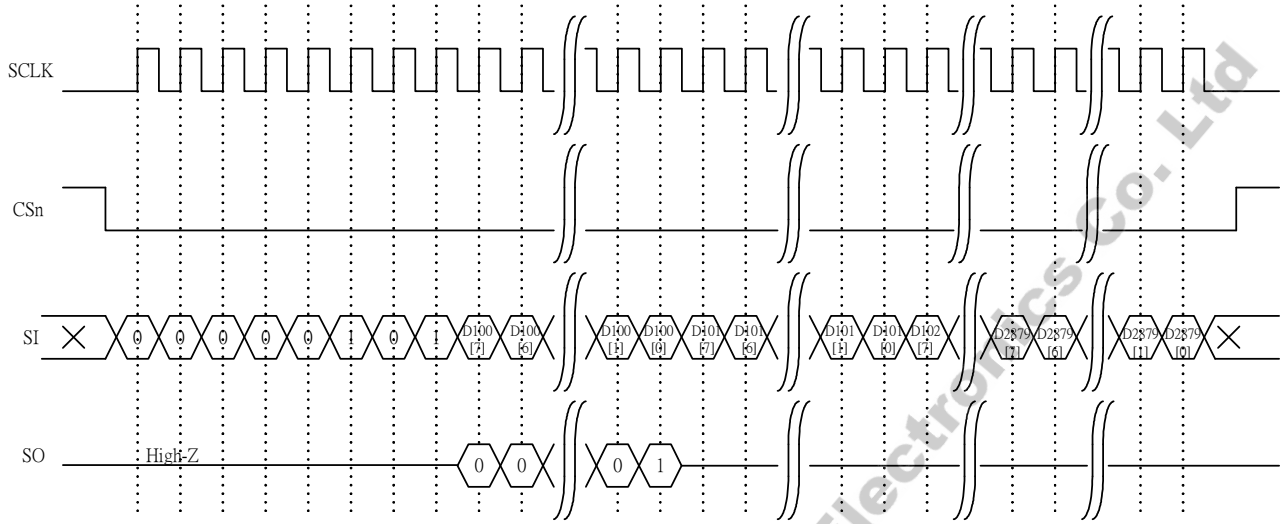


Figure 13-5: SPI Timing Diagram (IMGMEM Write: IMGIDX=0, NUMROWS=96, NUMCOLS=240)



Note: Address Byte is echoed back on SO during Write of first Byte .

Figure 13-6: SPI Timing Diagram (IMGMEM Write: IMGIDX=100, NUMROWS=96, NUMCOLS=240)



Note: Address Byte is echoed back on SO during Write of first Byte .

Figure 13-7: SPI Timing Diagram (IMGMEM Read: IMGIDX=0, NUMROWS=96, NUMCOLS=240)

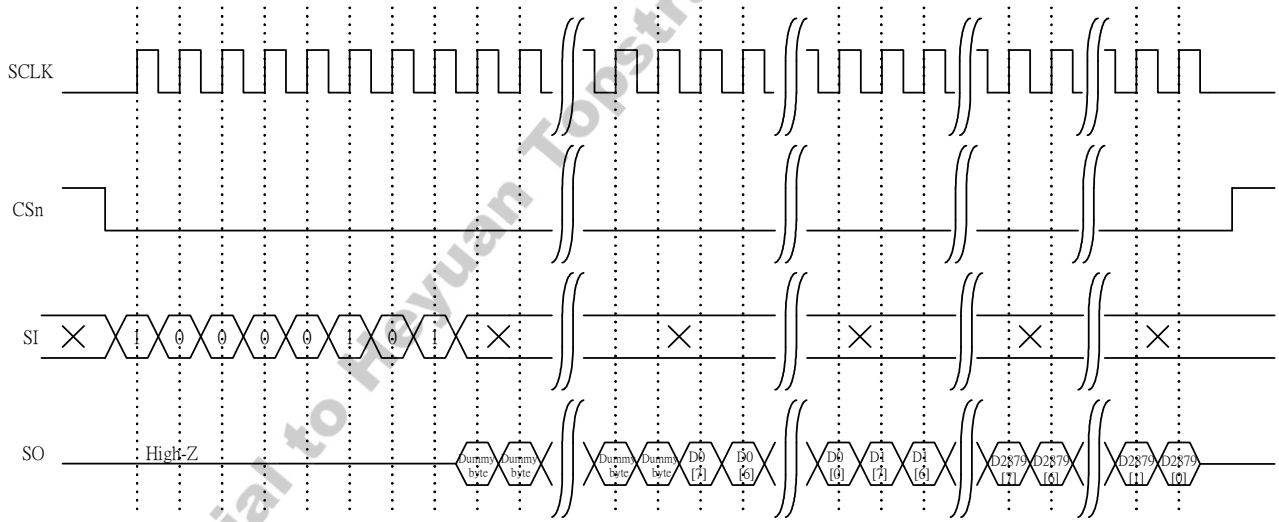


Figure 13-8: SPI Timing Diagram (IMGMEM Read: IMGIDX=100, NUMROWS=96, NUMCOLS=240)

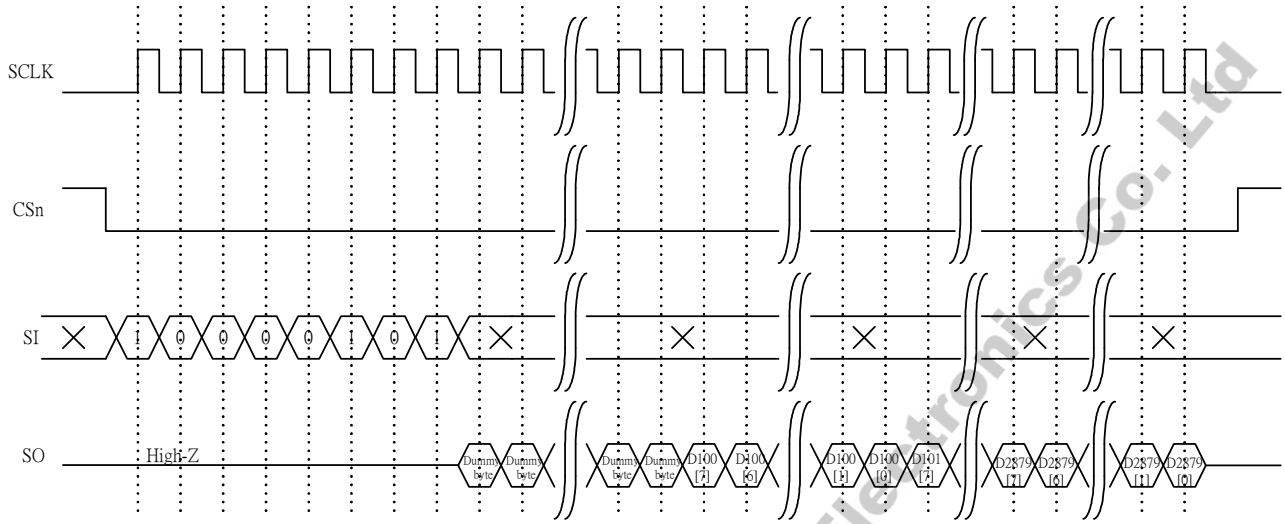
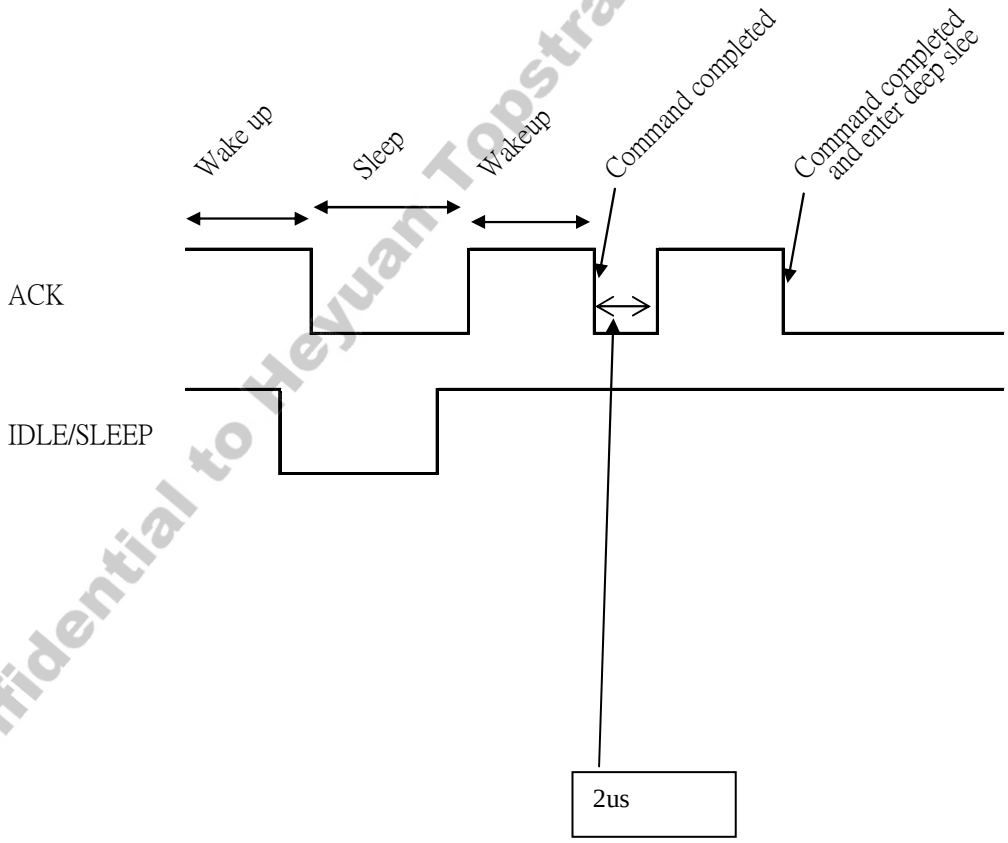
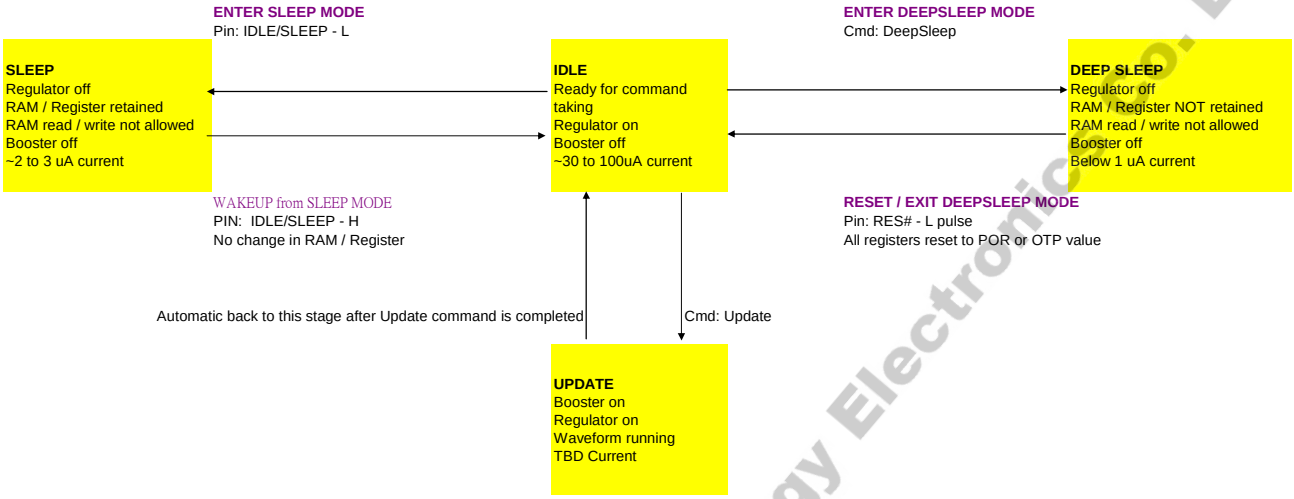


Figure 13-9: ACK pin output illustration



14 Definition of different power mode

Figure 14-1: Transition between different power mode

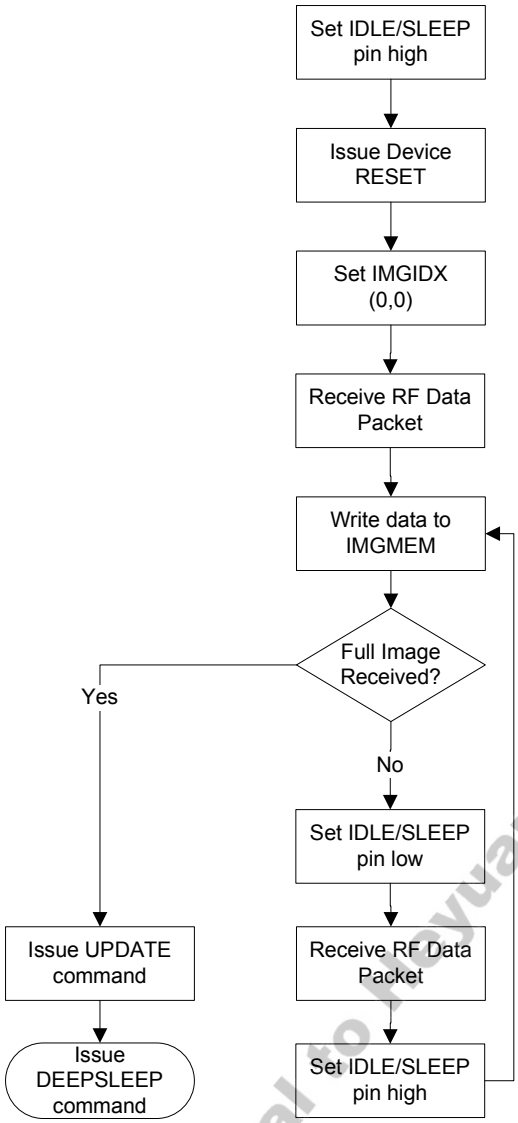


15 Hardware Reset Definition

If a hardware reset is performed then the behavior of the display is not defined. There is no guarantee that the display will be left in a DC-balanced state when a hardware reset is performed.

16 Standard UPDATE Flowchart

Figure 16-1: Standard update flow



17 Application circuit

Figure 17-1: Application circuit

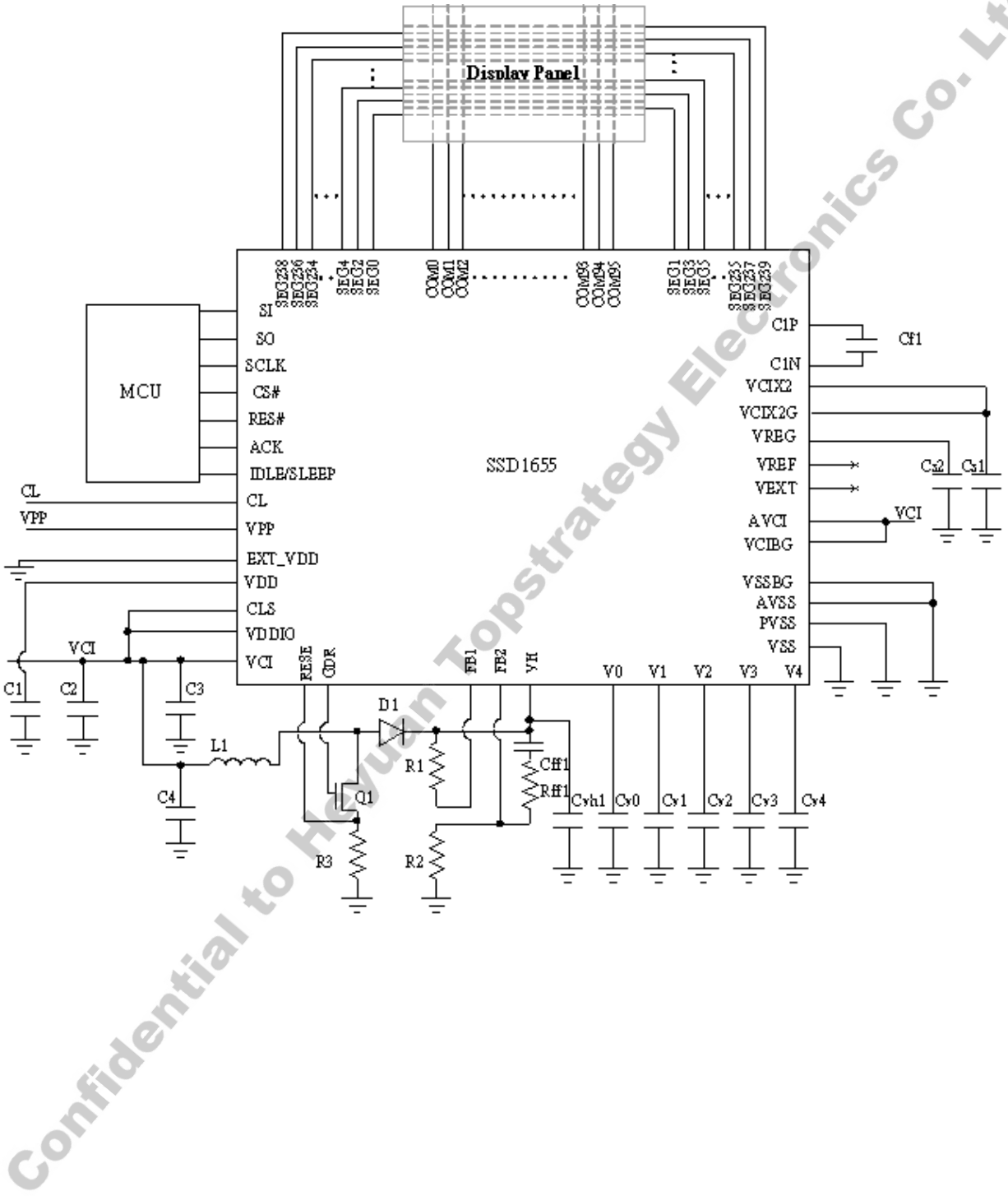


Table 17-1: Reference component selection

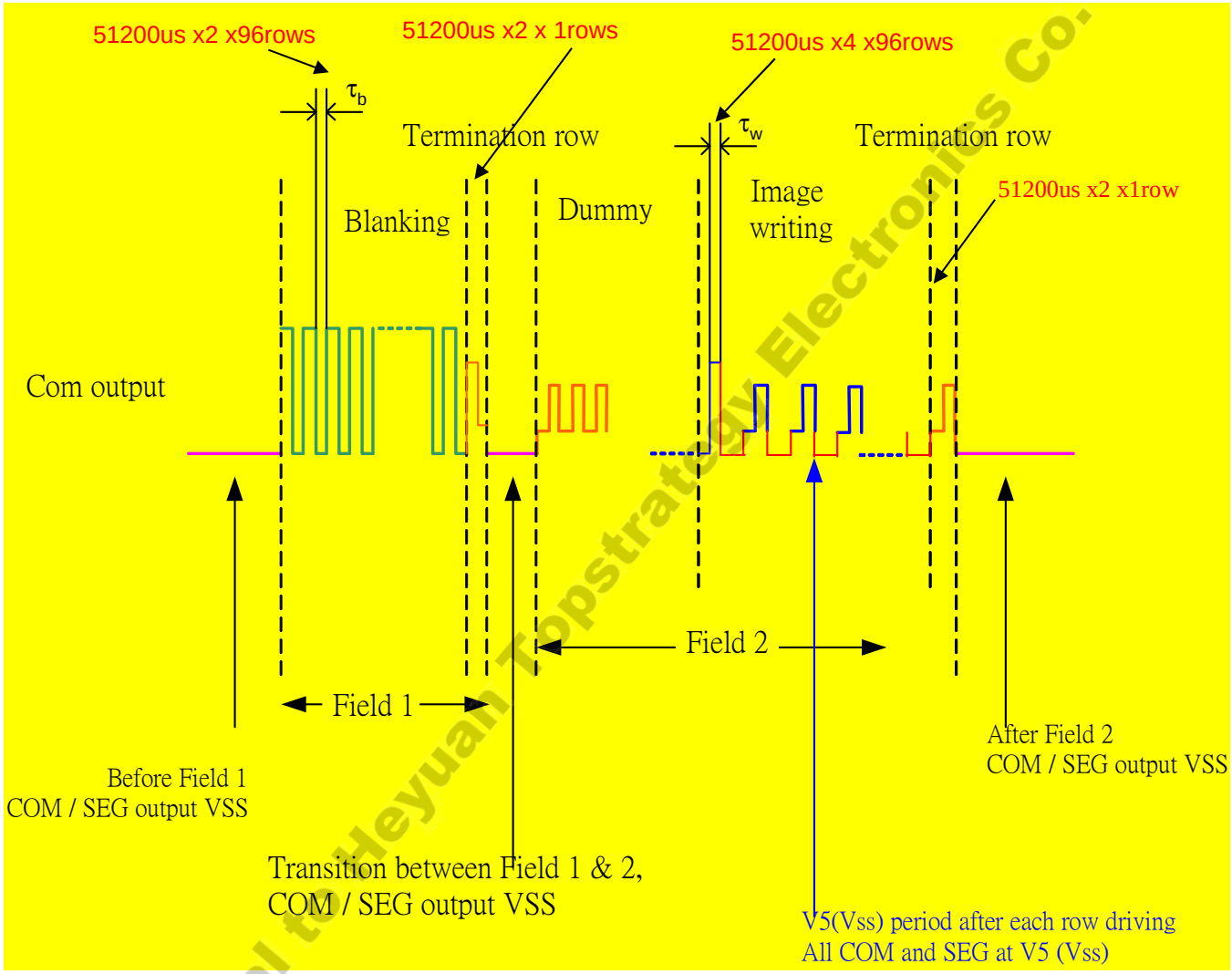
Item	Description	Destinator	Type	Value	Rating
1	Power MOSFET	Q1	MOS		50V
2	Schoktty Diode	D1	Diode		50V
3	Inductor	L1	Inductor	10uH	300mA
4	Current sensing resistor	R3	Resistor	1 ohm	1/10W
5	Resistor	R1	Resistor	Open	-
6	Resistor	R2	Resistor	Open	-
7	Capacitor for VDD	C1	Capacitor	0.1uF	6V
8	Capacitor for VDDIO	C2	Capacitor	0.1uF	6V
9	Capacitor for Booster VCI	C3	Capacitor	10uF	6V
10	Capacitor for Booster VCI	C4	Capacitor	10uF	6V
11	Feed forward capacitor	Cff1	Capacitor	NC (100pF)	50V
12	Resistor	Rff1	Resistor	NC(2K ohm)	-
13	Capacitor for VH	Cvh1	Capacitor	1uF	50V
14	Capacitor for V0	Cv0	Capacitor	0.47uF	50V
15	Capacitor bias buffer	Cv1	Capacitor	0.47uF	50V
16	Capacitor bias buffer	Cv2	Capacitor	0.47uF	50V
17	Capacitor bias buffer	Cv3	Capacitor	0.47uF	50V
18	Capacitor bias buffer	Cv4	Capacitor	0.47uF	50V
19	Capacitor for regulator	Cs2	Capacitor	0.47uF	6V
20	Capacitor for 2X charge pump output	Cs1	Capacitor	1uF	10V
21	Capacitor for 2X charge pump	Cf1	Capacitor	0.1uF	10V

Table 17-2: Power lines ITO resistance requirement for COG application

	Max ITO resistance requirement(unit: ohm)	
Pin Name	**For min VCI=VDDIO=2.0V**	**For min VCI=VDDIO=2.4V**
GDR	50	50
VH	30	30
V0	50	50
V1	100	100
V2	100	100
V3	100	100
V4	100	100
VDD	30	30
PVSS	20	20
VSS	30	30
AVSS	50	50
VSSBG	50	50
VPP	20	20
VDDIO	100	100
VCIBG	80	80
AVCI	80	80
VCI	30	30
VCIX2G	30	60
VCIX2	30	60
VREG	30	30
C1P	30	60
C1N	30	60

18 Default output

Figure 18-1: Default Common waveform with OTP blank (all 1)



The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard SJ/T 11363-2006 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)”. Hazardous Substances test report is available upon request.

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